IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

REQUEST FOR FILING
(RULE 53(b)(1))

For Design or Utility Applications

Rule 53(b)(1) PATENT APPLICATION: **(DO NOT USE FOR CIPs)**

☐ Continuation)
) application under 37 CFR 1.53(b)(1)
☒ Divisional)
application under 37 CFR 1.53(b)(1)
of pending prior application of

Group Art Unit: 2811

Examiner: TRAN, M.

Inventor(s): MANABE, et al.

Parent Appln. No.:	09	417,778	Atty. Dkt.	PM 273686	F00-219-US-DIV-3
	Series Code ⇧	Serial No. ⇧		New M#	Client Ref

Parent Filed: OCTOBER 14, 1999
This Appln. Filed: OCTOBER 2, 2000

Title: LIGHT-EMITTING SEMICONDUCTOR DEVICE USING GALLIUM NITRIDE GROUP COMPOUND

Hon. Commissioner of Patents
Washington, DC 20231

Date: October 2, 2000
(Parent Matter No. 258594)

Sir:

To effect the above-requested filing today:

1. **Attached** is a copy **(which must be filed)** of the prior application, including:

☒ Abstract
☒ Specification and claims (35 pages) **(must be attached)**
☒ Drawings **(must be attached if originally filed):** 11 sheet(s)/set: ☐ 1 set informal; ☒ Formal of size ☒ A4 ☐ 11"

1A. Always X one box, only:
(1) ☒ Copy of Signed declaration or oath as originally filed in prior application attached
(2) ☐ NO declaration or fee is enclosed; therefore, this is a filing under Rule 53(f).

2. ☐ This application is hereby filed by less than all of the inventors named in the prior application. Petition is hereby made requesting deletion as inventor(s) of the following who is/are **not** inventor(s) of the invention being claimed in this application (DELETE THE FOLLOWING INVENTOR(S)):

1. _____ 2. _____
3. _____ 4. _____
5. _____ 6. _____
7. _____ 8. _____

2.5 THE INVENTOR(S) FOR THIS NEW APPLICATION IS(ARE):

1. _____ 2. _____
3. _____ 4. _____
5. _____ 6. _____
7. _____ 8. _____

3. The entire disclosure of the prior application is considered as being part of the disclosure of the accompanying application and is hereby incorporated therein by reference thereto.

4. ☒ Priority is claimed under 35 U.S.C. 119/365 based on filing in JAPAN (country) of

	Application No.	Filing Date		Application No.	Filing Date
(1)	050209	28 FEB. 1990	(2)	050210	28 FEB. 1990
(3)	050211	28 FEB. 1990	(4)	050212	28 FEB. 1990
(5)			(6)		

a. ☐ _____ (No.) Certified copy/copies attached.
b. ☒ Certified copy/copies previously filed on FEBRUARY 27, 1991 in U.S. Application No. 07/661,304, filed on FEBRUARY 27, 1991.
series code ⇧ ⇧ serial no.
c. ☐ Certified copy/copies filed during International stage of PCT/ /
4. (a) ☐ Domestic priority is claimed from /, filed .
PCT/
(b) ☐ Benefit is claimed of Provisional Application No. 60/___, filed ___.

5. ☐ Prior application is assigned to (

by assignment recorded _____ Reel _____ Frame _____
(Date)

6. ☐ Attached is the following number of Assignments (including original and all later successive ones by different assignors): _____ and respective **new** Cover Sheets. (Do **NOT** file old cover sheets.)
(Assignments in parent **must be refiled** with new Cover Sheets in this continuing application if you want it/them recorded against the continuing application.)

Please return the recorded Assignment to the undersigned.

7. ☒ The power of attorney in the prior application is to PETER W. GOWDEY, REG. 25,872
(Name and Reg. No.)
whose current address is as in item 8 below.

a. ☐ Recognize as associate attorney _____
(Name, Reg. No. and Address)

8. **Address all future communications to Intellectual Property Group of Pillsbury Madison & Sutro LLP, Ninth Floor, East Tower 1100 New York Avenue, N.W., Washington, D.C. 20005-3918**

9. ☒ **Amend the specification** by inserting before the first line the sentence:--This is a ☐ continuation ☒ division of Application No. 09/417,778, filed OCTOBER 14, 1999
series code ⇧ ⇧ serial no.
(pending); which is a divisional of 08/956,950 filed Oct. 23, 1997 (allowed); which is a divisional of 08/556,232 filed Nov. 9, 1995 (patented); which is a continuation of 08/179,242, filed Jan. 10, 1994 (now abandoned); which is a divisional of 07/926,022, filed Aug. 7, 1997 (patented); which is a continuation of 07/661,304, filed Feb. 27, 1991 (now abandoned); the contents all of which are incorporated herein by reference. .--

9. (a) ☐ **Amend the specification** by inserting before the first line: --This application claims the benefit of Provisional Application No. 60/___, filed ___.--

10. ☐ It has been recently determined that this new continuing application is entitled to small entity status. Hence:
___(No.) Verified Statement(s) establishing "small entity" status under Rules 9 & 27 were/are:
☐ filed in above prior application (and hence applicable hereto)
☐ attached.

11. Petition to extend the life of the above prior application to at least the date hereof
(one box) ☒ is being concurrently filed in that prior application (Use Form PAT-111).
(must be) ☐ was previously filed in that prior application (Check length of prior extension).
(X'd) ☐ is not necessary for copendency (**Double check** before X'ing this box).

12. ☒ **INFORMATION DISCLOSURE STATEMENT:** Attached is Form PTO-1449 listing all of the documents cited by Applicant and the PTO in the parent application(s) relied upon under 35 USC 120 and referenced in item 9 above. Per Rule 98(d) copies of those documents are not required now. Please consider those documents and advise that they have been considered in this new application as by returning a copy of the enclosed Form PTO-1449 with the Examiner's initials in the left column per MPEP 609. .

13. ☐ Attached is a Rule 103(a) Petition to Suspend Action.

14. ☒ **PRELIMINARY AMENDMENT to be entered before fee calculation:** (Do not make amendments here except for correction of improper multiple dependencies or cancellation of whole claims or multiple dependencies for purpose of reducing the filing fee per MPEP §§ 506 and 607; do not cancel all claims).

PLEASE CANCEL CLAIMS 2-18.

FILING FEE

THE FOLLOWING FILING FEE IS BASED ON

->->->->CLAIMS AS FILED AND **CHANGED BY PRELIMINARY AMENDMENT IN ITEM 14**<-<-<-<-

NOTE: If box 1A2 is X'd, do not pay fees, but leave lines 15-22 and 27-32 blank.

PTO: PLEASE NOTE CLAIM CANCELLATIONS IF BOX 14 ABOVE IS X'D.

				Large/Small Entity		Fee Code
15. Basic Filing Fee . . . . . .Design Application				$310/$155		106/26
16. Basic Filing Fee . . . . . Not Design Application				$690/$345	~~+690~~ 710 cam	101/201
17. Total Effective Claims	1	minus 20 =	0	x $18/$9	+0	103/203
18. Independent Claims	1	minus 3 =	0	x $78/$39	+0	102/202
19. If any proper multiple dependent claim (ignore improper) is present,				$260/$130	+0	104/204
20.				**Subtotal =**	~~$690~~ 710 cam	
21. If "petition" box 13 above is X'd, add petition fee. $130					+0	122
21A. If box 6 above is X'd, add Assignment recording fee . . . . . $ 40					+0	581
22.				**TOTAL FILING FEE ATTACHED =**	~~$690~~ 710 cam	

(carry forward to Item 31)

23. ☐ ATTACHED:

24. ☒ Preliminary Amendment attached (to be entered after assigning Appln. No.)

25. ☐ The following PRELIMINARY AMENDMENT is to be entered after assigning Appln. No.:

26. **ADDITIONAL FEE CALCULATION FOR PRELIMINARY AMENDMENT PER BOXES 24/25**

	Claims remaining after amendment		Highest number previously paid for		Present Extra			Additional Fee	
							Large/Small Entity		File Code
27. Total Effective Claims	100	minus **	20	=	80	x $18/$9	=	$ 1,440	(103/203)
28. Independent Claims	6	minus ***	3	=	3	x $78/$39	=	+ ~~234~~ 240	(102/202)
29. If amendment enters proper multiple dependent claim(s) into this application for the first time, add (per application) ..... $260/$130								+ 0	(104/204)
30.							ADDITIONAL FEE	$ 0	
31.							plus **FEE** from item 22 on page 3	+ ~~890~~ 710 CAM	
32.							**TOTAL FEE ATTACHED**	$ ~~2,364~~ 2390 CAM	

33. *If the entry in this space is less than a entry in the next space, the "Present Extra" result is "0"

34. **If the "Highest number previously paid for" (see item 17 above) is less than 20, write "20" in this space

35. If the "Highest number previously paid for" (see item 18 above) is less than 3, write "3" in this space

Our Deposit Account No. 03-3975
Our Order No. 31317 (C#) | 273686 (M#)

CHARGE STATEMENT: Upon the filing of a Declaration pursuant to Rule 60(b) or 60(d), the Commissioner is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fee(s) filed, or asserted to be filed, or which should have been filed herewith or concerning any paper filed hereafter, and which may be required under Rules 16-18 (missing or insufficient fee only) now or hereafter relative to this application and the resulting Official document under Rule 20, or credit any overpayment, to our Account/Order Nos. shown above for which purpose a duplicate copy of this sheet is attached.
This CHARGE STATEMENT does not authorize charge of the issue fee until/unless an issue fee transmittal form is filed.

Pillsbury Madison & Sutro LLP
Intellectual Property Group

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Ninth Floor
Washington, DC 20005-3918
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PWG/WGB
Atty./Sec.

By Atty: Peter W. Gowdey **Reg. No.** 25,872
Sig: #41,844 for **Fax:** (202) 822-0944
Tel: (202) 861-3078

NOTE No. 1: File this Request in duplicate with 2 postcard receipts (PAT-103) & attachments
NOTE No. 2: Is extension in parent necessary for copendency? **DOUBLE CHECK** Item 11 above. If yes, printout Pat-111 and head it in parent.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

MANABE et al. Group Art Unit: 2811

Divisional of
Appln. No.: 09/417,778 Examiner: Tran, M.

Filed: Herewith

Title: LIGHT EMITTING SEMICONDUCTOR DEVICE USING GALLIUM NITRIDE GROUP COMPOUND

October 2, 2000

PRELIMINARY AMENDMENT

Honorable Commissioner of
Patents and Trademarks,
Washington, DC 20231

Sir:

Kindly enter the following preliminary amendments.

IN THE TITLE:

Please change the title to --A METHOD FOR MANUFACTURING A GALLIUM NITRIDE GROUP COMPOUND SEMICONDUCTOR--.

IN THE CLAIMS:

Please cancel claim 1 and add the attached new claims 19-118.

--19. A method for producing a gallium nitride group compound semiconductor by using an organometallic compound vapor phase epitaxy, comprising the steps of:

setting a mixing ratio of a silicon-containing gas and other raw material gases during said vapor phase epitaxy at a desired value in a range which increases substantially in proportion to a conductivity (1/resistivity) of said gallium nitride group compound semiconductor so as to control conductivity (1/resistivity) of said gallium nitride group compound semiconductor at a desired value; and

forming said gallium nitride group compound semiconductor by feeding said silicon-containing gas and other raw material gases at a mixing ratio set above.

20. A method for producing a gallium nitride group compound semiconductor by using an organometallic compound vapor phase epitaxy, comprising the steps of:

setting a mixing ratio of a silicon-containing gas and other raw material gases during said vapor phase epitaxy at a desired value in a range which increases substantially in proportion to an electron concentration of said gallium nitride group compound semiconductor so as to control a carrier concentration of said gallium nitride group compound semiconductor at a desired value; and

forming said gallium nitride group compound semiconductor by feeding said silicon-containing gas and other raw material gases at a mixing ratio set above.

21. A method for producing a gallium nitride group compound semiconductor according to claim 19, wherein said gallium nitride group compound semiconductor is $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$).

22. A method for producing a gallium nitride group compound semiconductor according to claim 20, wherein said gallium nitride group compound semiconductor is $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$).

23. A method for producing a gallium nitride group compound semiconductor according to claim 19, wherein said gallium nitride group compound semiconductor is GaN.

24. A method for producing a gallium nitride group compound semiconductor according to claim 20, wherein said gallium nitride group compound semiconductor is GaN.

25. A method for producing a gallium nitride group compound semiconductor according to claim 19, wherein said conductivity (1/resistivity) is not less than 3.3/Ωcm.

26. A method for producing a gallium nitride group compound semiconductor according to claim 21, wherein said conductivity (1/resistivity) is not less than 3.3/Ωcm.

27. A method for producing a gallium nitride group compound semiconductor according to claim 23, wherein said conductivity (1/resistivity) is not less than 3.3/Ωcm.

28. A method for producing a gallium nitride group compound semiconductor according to claim 20, wherein said electron concentration is not less than $6 \times 10^{16}/cm^3$.

29. A method for producing a gallium nitride group compound semiconductor according to claim 22, wherein said electron concentration is not less than $6 \times 10^{16}/cm^3$.

30. A method for producing a gallium nitride group compound semiconductor according to claim 24, wherein said electron concentration is not less than $6 \times 10^{16}/cm^3$.

31. A method for producing a gallium nitride group compound semiconductor according to claim 19, wherein said conductivity (1/resistivity) is ranging from 3.3/Ωcm to 1.3 x $1O^2$/Ωcm.

32. A method for producing a gallium nitride group compound semiconductor according to claim 21, wherein said conductivity (1/resistivity) is ranging from 3.3/Ωcm to 1.3 x $1O^2$/Ωcm.

33. A method for producing a gallium nitride group compound semiconductor according to claim 23, wherein said conductivity (1/resistivity) is ranging from 3.3/Ωcm to 1.3 x 10^2/Ωcm.

34. A method for producing a gallium nitride group compound semiconductor according to claim 20, wherein said electron concentration is ranging from 6 x 10^{16}/cm^3 to 3 x 10^{18}/cm^3.

35. A method for producing a gallium nitride group compound semiconductor according to claim 22, wherein said electron concentration is ranging from 6 x 10^{16}/cm^3 to 3 x 10^{18}/cm^3.

36. A method for producing a gallium nitride group compound semiconductor according to claim 24, wherein said electron concentration is ranging from 6 x 10^{16}/cm^3 to 3 x 10^{18}/cm^3.

37. A method for producing a gallium nitride group compound semiconductor according to claim 19, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

38. A method for producing a gallium nitride group compound semiconductor according to claim 20, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

39. A method for producing a gallium nitride group compound semiconductor according to claim 21, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

40. A method for producing a gallium nitride group compound semiconductor according to claim 22, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

41. A method for producing a gallium nitride group compound semiconductor according to claim 25, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

42. A method for producing a gallium nitride group compound semiconductor according to claim 28, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

43. A method for producing a gallium nitride group compound semiconductor according to claim 31, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

44. A method for producing a gallium nitride group compound semiconductor according to claim 34, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

45. A method for producing a gallium nitride group compound semiconductor according to claim 37, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

46. A method for producing a gallium nitride group compound semiconductor according to claim 38, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

47. A method for producing a gallium nitride group compound semiconductor according to claim 39, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

48. A method for producing a gallium nitride group compound semiconductor according to claim 40, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

49. A method for producing a gallium nitride group compound semiconductor according to claim 41, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

50. A method for producing a gallium nitride group compound semiconductor according to claim 42, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

51. A method for producing a gallium nitride group compound semiconductor according to claim 43, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

52. A method for producing a gallium nitride group compound semiconductor according to claim 44, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

53. A method for producing a gallium nitride group compound semiconductor by an organometallic compound vapor phase epitaxy, comprising the steps of:

setting a supplying rate of silicon (Si) to gallium (Ga) in a reaction chamber during said vapor phase epitaxy at a desired value in a range from 0.1 to 3 as a converted values so as to control a conductivity (1/resistivity) of said gallium nitride group compound semiconductor at a desired value, where said values 0.1 and 3 are the values obtained from gas flow rates, in case that an amount of said gallium (Ga) is converted into a flow rate of hydrogen bubbling trimethyl gallium (TMG) at a temperature of -15°C and an amount of said silicon (Si) is converted into a flow rate of a gas diluted to 0.86 ppm.

54. A method for producing a gallium nitride group compound semiconductor by an organometallic compound vapor phase epitaxy, comprising the steps of:

setting a supplying rate of silicon (Si) to NH_3 in a reaction chamber during said vapor phase epitaxy at a desired value in a range from 8.6×10^{-10} to 2.6×10^{-8}, so as to control a conductivity (1/resistivity) of said gallium nitride group compound semiconductor at a desired value.

55. A method for producing a gallium nitride group compound semiconductor by an organometallic compound vapor phase epitaxy, comprising the steps of:

setting a supplying rate of silicon (Si) to gallium (Ga) in a reaction chamber during said vapor phase epitaxy at a desired value in a range from 0.1 to 3 as a converted values so as to control a carrier concentration of said gallium nitride group compound semiconductor at a desired value, where said values 0.1 and 3 are the values obtained from gas flow rates, in case that an amount of said gallium (Ga) is converted into a flow rate of hydrogen bubbling

trimethyl gallium (TMG) at a temperature of -15°C and an amount of said silicon (Si) is converted into a flow rate of a gas diluted to 0.86 ppm.

56. A method for producing a gallium nitride group compound semiconductor by an organometallic compound vapor phase epitaxy, comprising the steps of:

setting a supplying rate of silicon (Si) to NH_3 in a reaction chamber during said vapor phase epitaxy at a desired value in a range from 8.6×10^{-10} to 2.6×10^{-8}, so as to control a carrier concentration of said gallium nitride group compound semiconductor at a desired value.

57. A method for producing a gallium nitride group compound semiconductor according to claim 53, wherein said gallium nitride group compound semiconductor is $Al_XGa_{1-X}N$ ($0 \leq x \leq 1$).

58. A method for producing a gallium nitride group compound semiconductor according to claim 54, wherein said gallium nitride group compound semiconductor is $Al_XGa_{1-X}N$ ($0 \leq x \leq 1$).

59. A method for producing a gallium nitride group compound semiconductor according to claim 55, wherein said gallium nitride group compound semiconductor is $Al_XGa_{1-X}N$ ($0 \leq x \leq 1$).

60. A method for producing a gallium nitride group compound semiconductor according to claim 56, wherein said gallium nitride group compound semiconductor is $Al_XGa_{1-X}N$ ($0 \leq x \leq 1$).

61. A method for producing a gallium nitride group compound semiconductor according to claim 53, wherein said gallium nitride group compound semiconductor is GaN.

62. A method for producing a gallium nitride group compound semiconductor according to claim 54, wherein said gallium nitride group compound semiconductor is GaN.

63. A method for producing a gallium nitride group compound semiconductor according to claim 55, wherein said gallium nitride group compound semiconductor is GaN.

64. A method for producing a gallium nitride group compound semiconductor according to claim 56, wherein said gallium nitride group compound semiconductor is GaN.

65. A method for producing a gallium nitride group compound semiconductor according to claim 53, wherein said conductivity (1/resistivity) is not less than 3.3/Ωcm.

66. A method for producing a gallium nitride group compound semiconductor according to claim 54, wherein said conductivity (1/resistivity) is not less than 3.3/Ωcm.

67. A method for producing a gallium nitride group compound semiconductor according to claim 57, wherein said conductivity (1/resistivity) is not less than 3.3/Ωcm.

68. A method for producing a gallium nitride group compound semiconductor according to claim 58, wherein said conductivity (1/resistivity) is not less than 3.3/Ωcm.

69. A method for producing a gallium nitride group compound semiconductor according to claim 61, wherein said conductivity (1/resistivity) is not less than 3.3/Ωcm.

70. A method for producing a gallium nitride group compound semiconductor according to claim 62, wherein said conductivity (1/resistivity) is not less than 3.3/Ωcm.

71. A method for producing a gallium nitride group compound semiconductor according to claim 55, wherein said electron concentration is not less than $6 \times 10^{16}/cm^3$.

72. A method for producing a gallium nitride group compound semiconductor according to claim 56, wherein said electron concentration is not less than $6 \times 10^{16}/cm^3$.

73. A method for producing a gallium nitride group compound semiconductor according to claim 59, wherein said electron concentration is not less than $6 \times 10^{16}/cm^3$.

74. A method for producing a gallium nitride group compound semiconductor according to claim 60, wherein said electron concentration is not less than $6 \times 10^{16}/cm^3$.

75. A method for producing a gallium nitride group compound semiconductor according to claim 53, wherein said conductivity (1/resistivity) is ranging from 3.3/Ωcm to 1.3×10^2/Ωcm.

76. A method for producing a gallium nitride group compound semiconductor according to claim 54, wherein said conductivity (1/resistivity) is ranging from 3.3/Ωcm to 1.3×10^2/Ωcm.

77. A method for producing a gallium nitride group compound semiconductor according to claim 57, wherein said conductivity (1/resistivity) is ranging from 3.3/Ωcm to 1.3×10^2/Ωcm.

78. A method for producing a gallium nitride group compound semiconductor according to claim 58, wherein said conductivity (1/resistivity) is ranging from 3.3/Ωcm to 1.3×10^2/Ωcm.

79. A method for producing a gallium nitride group compound semiconductor according to claim 61, wherein said conductivity (1/resistivity) is ranging from 3.3/Ωcm to 1.3×10^2/Ωcm.

80. A method for producing a gallium nitride group compound semiconductor according to claim 62, wherein said conductivity (1/resistivity) is ranging from 3.3/Ωcm to 1.3×10^2/Ωcm.

81. A method for producing a gallium nitride group compound semiconductor according to claim 55, wherein said electron concentration is ranging from 6×10^{16}/cm^3 to 3×10^{18}/cm^3.

82. A method for producing a gallium nitride group compound semiconductor according to claim 56, wherein said electron concentration is ranging from 6×10^{16}/cm^3 to 3×10^{18}/cm^3.

83. A method for producing a gallium nitride group compound semiconductor according to claim 59, wherein said electron concentration is ranging from 6 x $10^{16}/cm^3$ to 3 x $10^{18}/cm^3$.

84. A method for producing a gallium nitride group compound semiconductor according to claim 60, wherein said electron concentration is ranging from 6 x $10^{16}/cm^3$ to 3 x $10^{18}/cm^3$.

85. A method for producing a gallium nitride group compound semiconductor according to claim 63, wherein said electron concentration is ranging from 6 x $10^{16}/cm^3$ to 3 x $10^{18}/cm^3$.

86. A method for producing a gallium nitride group compound semiconductor according to claim 64, wherein said electron concentration is ranging from 6 x $10^{16}/cm^3$ to 3 x $10^{18}/cm^3$.

87. A method for producing a gallium nitride group compound semiconductor according to claim 53, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

88. A method for producing a gallium nitride group compound semiconductor according to claim 54, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

89. A method for producing a gallium nitride group compound semiconductor according to claim 55, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

90. A method for producing a gallium nitride group compound semiconductor according to claim 56, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

91. A method for producing a gallium nitride group compound semiconductor according to claim 57, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

92. A method for producing a gallium nitride group compound semiconductor according to claim 58, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

93. A method for producing a gallium nitride group compound semiconductor according to claim 59, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

94. A method for producing a gallium nitride group compound semiconductor according to claim 60, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

95. A method for producing a gallium nitride group compound semiconductor according to claim 61, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

96. A method for producing a gallium nitride group compound semiconductor according to claim 62, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

97. A method for producing a gallium nitride group compound semiconductor according to claim 63, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

98. A method for producing a gallium nitride group compound semiconductor according to claim 64, wherein said gallium nitride group compound semiconductor is formed on or above a buffer layer which is formed on a sapphire substrate.

99. A method for producing a gallium nitride group compound semiconductor according to claim 87, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

100. A method for producing a gallium nitride group compound semiconductor according to claim 88, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

101. A method for producing a gallium nitride group compound semiconductor according to claim 89, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

102. A method for producing a gallium nitride group compound semiconductor according to claim 90, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

103. A method for producing a gallium nitride group compound semiconductor according to claim 91, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

104. A method for producing a gallium nitride group compound semiconductor according to claim 92, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

105. A method for producing a gallium nitride group compound semiconductor according to claim 93, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

106. A method for producing a gallium nitride group compound semiconductor according to claim 94, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

107. A method for producing a gallium nitride group compound semiconductor according to claim 95, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

108. A method for producing a gallium nitride group compound semiconductor according to claim 96, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

109. A method for producing a gallium nitride group compound semiconductor according to claim 97, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

110. A method for producing a gallium nitride group compound semiconductor according to claim 98, wherein said buffer layer is formed on said sapphire substrate by using an organometallic compound vapor phase epitaxy at a growth temperature lower than that of said gallium nitride group compound semiconductor.

111. A method for producing a gallium nitride group compound semiconductor according to claim 19, wherein silicon-containing gas is silane (SiH_4).

112. A method for producing a gallium nitride group compound semiconductor according to claim 20, wherein silicon-containing gas is silane (SiH_4).

113. A method for producing a gallium nitride group compound semiconductor according to claim 53, wherein silicon-containing gas is silane (SiH_4).

114. A method for producing a gallium nitride group compound semiconductor according to claim 54, wherein silicon-containing gas is silane (SiH_4).

115. A method for producing a gallium nitride group compound semiconductor according to claim 55, wherein silicon-containing gas is silane (SiH_4).

116. A method for producing a gallium nitride group compound semiconductor according to claim 56, wherein silicon-containing gas is silane (SiH_4).

117. A method for producing a gallium nitride group compound semiconductor according to claim 63, wherein said electron concentration is not less than $6 \times 10^{16}/cm^3$.

118. A method for producing a gallium nitride group compound semiconductor according to claim 64, wherein said electron concentration is not less than $6 \times 10^{16}/cm^3$.--

REMARKS

Please enter the above amendments prior to examination. If the Examiner has any questions regarding the foregoing, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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LIGHT-EMITTING SEMICONDUCTOR DEVICE USING GALLIUM NITRIDE GROUP COMPOUND

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a light-emitting semiconductor device using gallium nitride group compound which emits a blue light.

2. Description of the Prior Art

It is known that GaN compound semiconductor can be made into a light-emitting semiconductor device, such as a light-emitting diode (LED), which emits a blue light. The GaN compound semiconductor attracts attention because of its high light-emitting efficiency resulting from direct transition and of its ability to emit a blue light which is one of three primary colors.

The light-emitting diode manufactured from the GaN compound semiconductor is composed of an n-layer and an i-layer grown thereon. The n-layer of the GaN compound semiconductor with n-type conduction is directly grown on a surface of a sapphire substrate or grown on a buffer layer of aluminum nitride formed on the substrate. The i-layer of insulating (i-type) GaN compound semiconductor doped with p-type impurities is grown on the n-layer. (See Japanese Patent Laid-open

Nos. 119196/1987 and 188977/1988.) The light-emitting diode of this structure has room for improvement in luminous intensity. In addition, it comprises no p-n junction but it is made by joining the i-layer and n-layer.

An electric property of the GaN compound semiconductor shows inherently n-type conduction even though it is not deliberately doped with n-type impurities, and unlike silicon and similar semiconductors, when it is doped with zinc of p-type impurities, the electric property shows not p-type conduction but insulation. Moreover, the production of n-type GaN involves many difficulties in controlling conductivity.

SUMMARY OF THE INVENTION

It is the first object of the present invention to improve a luminous efficiency of a GaN group light-emitting diode.

It is the second object of the present invention to provide a new layer structure which improves a luminous efficiency of a GaN group light-emitting diode.

It is the third object of the present invention to provide a technology for production of n-type GaN group compound semiconductor in which conductivity is

easily controlled.

After experience in the manufacture of the above-mentioned GaN light-emitting diode, the present inventors established a technology for a vapor phase epitaxy of the GaN group semiconductor with organometal compound. This technology enables a production of a gas-phase grown GaN layer of high purity. In other words, this technology provides n-type GaN with high resistivity without doping with impurities, unlike the conventional technology which provides n-type GaN with low resistivity when no doping is performed.

The first feature of the invention;

The first feature of the present invention resides in a light-emitting semiconductor device composed of an n-layer of n-type gallium nitride group compound semiconductor ($Al_XGa_{1-X}N$; inclusive of x=0) and an i-layer of insulating (i-type) gallium nitride compound semiconductor ($Al_XGa_{1-X}N$; inclusive of x=0) doped with p-type impurities, in which the n-layer is of double-layer structure including an n-layer of low carrier concentration and an n^+-layer of high carrier concentration, the former being adjacent to the i-layer.

According to the present invention, the n-layer of low carrier concentration should preferably have a carrier concentration of 1 x $10^{14}/cm^3$ to 1 x $10^{17}/cm^3$

and have a thickness of 0.5 to 2 μm. In case that the carrier concentration is higher than 1 x $10^{17}/cm^3$, the luminous intensity of the light-emitting diode decreases. In case that the carrier concentration is lower than 1 x $10^{14}/cm^3$, since the series resistance of the light-emitting diode increases, an amount of heat generated in the n-layer increases when a constant current is supplied to it. In case that the layer thickness is greater than 2 μm, since the series resistance of the light-emitting diode increases, the amount of heat generated in the n-layer increases when the constant current is supplied to it. In case that the layer thickness is smaller than 0.5 μm, the luminous intensity of the light-emitting diode decreases.

In addition, the n^+-layer of high carrier concentration should preferably contain a carrier concentration of 1 x $10^{17}/cm^3$ to 1 x $10^{19}/cm^3$ and have a thickness of 2-10 μm. In case that the carrier concentration is higher than 1 x $10^{19}/cm^3$, the n^+-layer is poor in crystallinity. In case that the carrier concentration is lower than 1 x $10^{17}/cm^3$, since the series resistance of the light-emitting diode increases, an amount of heat generated in the n^+-layer increases when a constant current is supplied to it. In case that the layer thickness is greater than 10 μm, the

substrate of the light-emitting diode warps. In case that the layer thickness is smaller than 2 μm, since the series resistace of the light-emitting diode increases, the amount of heat generated in the n^+-layer increases when the constant current is supplied to it.

In the first feature of the present invention, it is possible to increase an intensity of blue light emitted from the light-emitting diode by making the n-layer in double-layer structure including an n-layer of low carrier concentration and an n^+-layer of high carrier concentration, the former being adjacent to the i-layer. In other words, the n-layer as a whole has a low electric resistance owing to the n^+-layer of high carrier concentration, and hence the light-emitting diode has low series resistance and generates less heat when a constant current is supplied to it. The n-layer adjacent to the i-layer has a lower carrier concentration or higher purity so that it contains a smaller amount of impurity atoms which are deleterious to the emission of blue light from the light-emission region (i-layer and its vicinity). Due to the above-mentioned functions, the light-emitting diode of the present invention emits a blue light of higher intensity.

The second feature of the invention

The second feature of the present invention resides in a light-emitting semiconductor device composed of an n-layer of n-type gallium nitride compound semiconductor ($Al_XGa_{1-X}N$; inclusive of x=0) and an i-layer of i-type gallium nitride compound semiconductor ($Al_XGa_{1-X}N$; inclusive of x=0) doped with p-type impurities, in which the i-layer is of double-layer structure including an i_L-layer containing p-type impurities in comparatively low concentration and an i_H-layer containing p-type impurities in comparatively high concentration, the former being adjacent to the n-layer.

According to the present invention, the i_L-layer of low impurity concentration should preferably contain the impurities in concentration of 1 x $10^{16}/cm^3$ to 5 x $10^{19}/cm^3$ and have a thickness of 0.01 to 1 μm. In case that impurity concentration is higher than 5 x $10^{19}/cm^3$, since the series resistance of the light-emitting diode increases, an initial voltage to start emitting light at increases. In case that the impurity concentration is lower than 1 x $10^{16}/cm^3$, the semiconductor of the i_L-layer shows n-type conduction. In case that the layer thickness is greater than 1 μm, since the series resistance of the light-emitting diode increases, the initial voltage to start emitting light

at increases. In case that the layer thickness is smaller than 0.01 μm, the light-emitting diode has the same structure as that of the conventional one.

In addition, the i_H-layer of high impurity concentration should preferably contain the impurities in concentration of 1 x $10^{19}/cm^3$ to 5 x $10^{20}/cm^3$ and have a thickness of 0.02 to 0.3 μm. In case that the impurity concentration is higher than 5 x $10^{20}/cm^3$, the semiconductor of the i_H-layer is poor in crystallinity. In case that the impurity concentration is lower than 1 x $10^{19}/cm^3$, the luminous intensity of the light-emitting diode decreases. In case that the layer thickness is greater than 0.3 μm, since the series resistance of the light-emitting diode increases, an initial voltage to start emitting light at increases. In case that the layer thickness is smaller than 0.02 μm, the i-layer is subject to breakage.

In the second feature of the present invention, it is possible to increase an intensity of blue light emitted from the light-emitting diode by making the i-layer in double-layer structure including an i_L-layer containing p-type impurities in comparatively low concentration and an i_H-layer containing p-type impurities in comparatively high concentration, the former being adjacent to the n-layer. In other words,

this structure (in which the i-layer adjacent to the n-layer is the i_L-layer of low impurity concentration) enables electrons to be injected from the n-layer into the i_H-layer of high impurity concentration without being trapped in the i_L-layer and its vicinity. Therefore, this structure enables electrons to pass through the i_L-layer of low impurity concentration , which is poor in luminous efficacy, adjacent to the n-layer, and to reach the i_H-layer of high impurity concentration in which electrons emit light with a high efficiency.

The third feature of the invention

The third feature of the present invention resides in a light-emitting semiconductor device composed of an n-layer of n-type gallium nitride compound semiconductor ($Al_XGa_{1-X}N$; inclusive of x=0) and an i-layer of i-type gallium nitride compound semiconductor ($Al_XGa_{1-X}N$; inclusive of x=0) doped with p-type impurities, in which the n-layer is of double-layer structure including an n-layer of low carrier concentration and an n^+-layer of high carrier concentration, the former being adjacent to the i-layer, and the i-layer is of double-layer structure including an i_L-layer containing p-type impurities in

comparatively low concentration and an i_H-layer containing p-type impurities in comparatively high concentration, the former being adjacent to the n-layer.

The third feature of the present invention is a combination of the first feature (the n-layer of double layer structure) and the second feature (the i-layer of double layer structure). Therefore, the n-layer of low carrier concentration, the n^--layer of high carrier concentration, the i_L-layer of low impurity concentration, and the i_H-layer of high impurity concentration should correspond to the respective layers as the first and second features. The carrier concentration and layer thickness are defined in the same manner as in the first and second features.

In the third feature of the present invention, it is possible to increase an intensity of blue light from the light-emitting diode by making the n-layer in double-layer structure including an n-layer of low carrier concentration and an n^+-layer of high carrier concentration, the former being adjacent to the i-layer, and also by making the i-layer in double-layer structure including an i_L-layer containing p-type impurities in comparatively low concentration and an i_H-layer containing p-type impurities in comparatively high concentration, the former being adjacent to the n-layer.

In other words, the n-layer as a whole has a low electric resistance owing to the n^+-layer of high carrier concentration, which makes it possible to apply an effective voltage to the junction between the i_L-layer and n-layer of low carrier concentration. Having a low carrier concentration, the n-layer adjacent to the i_L-layer does not permit non-light-emitting impurity atoms to diffuse into the i_L-layer. In addition, this structure (in which the i-layer adjacent to the n-layer is the i_L-layer of low impurity concentration) permits electrons to be injected from the n-layer into the i_H-layer of high impurity concentration without being trapped in the i_L-layer. Therefore, this structure permits electrons to pass through the i_L-layer of low impurity concentration, which is poor in luminous efficacy, adjacent to the n-layer, and to reach the i_H-layer of high impurity concentration in which electrons emit light with a high efficiency.

For this reason, the light-emitting diode of the present invention has a much higher luminous efficacy than the one having the conventional simple i-n junction.

The fourth feature of the invention

The fourth feature of the present invention resides in a method of producing an n-type gallium

nitride compound semiconductor ($Al_xGa_{1-x}N$; inclusive of x=0) from organometal compound by vapor phase epitaxy. This method comprises a step of feeding a silicon-containing gas and other raw material gases together at a proper mixing ratio so that the conductivity of the compound semiconductor is desirably controlled. The mixing ratio is adjusted such that silicon enters the layer of gallium nitride compound semiconductor grown by vapor phase epitaxy and functions as the donor therein. Thus it is possible to vary the conductivity of the n-type layer by adjusting the mixing ratio.

The fifth feature of the invention

The fifth feature of the present invention resides in a method for producing a light-emitting semiconductor device. The method comprises two steps. The first step involves growing an n^+-layer of high carrier concentration (which is an n-type gallium nitride compound semiconductor ($Al_xGa_{1-x}N$; inclusive of x=0) having a comparatively high conductivity) by vapor phase epitaxy from organometal compound. The vapor phase epitaxy is accomplished on a sapphire substrate having a buffer layer of aluminum nitride by feeding a silicon-containing gas and other raw material gases together at a proper mixing ratio. The second step

involves growing an n-layer of low carrier concentration (which is an n-type gallium nitride compound semiconductor ($Al_XGa_{1-X}N$; inclusive of x=0) having a comparatively low conductivity) by vapor phase epitaxy from organometal compound. The vapor phase epitaxy is accomplished on the n^+-layer formed by the first step by feeding raw material gases excluding the silicon-containing gas. The n-layer of double-layer structure can be produced by properly controlling the mixing ratio of a silicon-containing gas and other raw material gases.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing a structure of a light-emitting diode shown as Example 1 of the present invention.

Figs. 2 to 7 are sectional views illustrating processes for producing a light-emitting diode shown as to Example 1 of the present invention.

Fig. 8 is a diagram showing relationship between a carrier concentration of an n-layer of low carrier concentration and intensity or wavelength of emitted light with respect to a light-emitting diode shown as Example 1 of the present invention.

Fig. 9 is a diagram showing a structure of a

light-emitting diode shown as Example 2 of the present invention.

Figs. 10 to 15 are sectional views illustrating processes for producing a light-emitting diode shown as Example 2 of the present invention.

Fig. 16 is a diagram showing relationship between an impurity concentration of an i_H-layer of high impurity concentration and intensity or wavelength of emitted light with respect to a light-emitting diode shown as Example 2 of the present invention.

Fig. 17 is a diagram showing a structure of a light emitting diode shown as Example 3 of the present invention.

Figs. 18 to 23 are sectional views illustrating processes for producing a light-emitting diode shown as Example 3 of the present invention.

Fig. 24 is a diagram showing relationship between a carrier concentration of an n-layer of low carrier concentration and intensity or wavelength of emitted light with respect to a light-emitting diode shown as Example 3 of the present invention.

Fig. 25 is a diagram showing relationship between an impurity concentration of an i_H-layer of high impurity concentration and intensity or wavelength of emitted light with respect to a light-emitting diode

shown as Example 3 of the present invention.

Fig. 26 is a diagram showing the relationship between a flow rate of silane gas and electrical properties of an n-layer formed by vapor phase epitaxy in a process shown as Example 4 of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention will be described in more detail with reference to the following examples.

Example 1

In Fig. 1 there is shown a light-emitting diode 10 which has a sapphire substrate 1 on which is formed a buffer layer of 500 Å thick AlN. On the buffer layer 2 are consecutively formed an n^+-layer 3 of high carrier concentration of 2.2 μm thick GaN and an n-layer 4 of low carrier concentration of 1.5 μm thick GaN. And an i-(insulating) layer 6 of 0.2 μm thick GaN is formed on the n-layer 4. Aluminum electrodes 7 and 8 are connected to the i-layer 6 and n^+-layer 3, respectively.

This light-emitting diode 10 was produced by metalorganic vapor phase epitaxy in the following manner. (This process is referred to as MOVPE hereinafter.)

The gases employed in this process are NH_3, H_2

(as carrier gas), trimethyl gallium ($Ga(CH_3)_3$) (TMG hereinafter), trimethyl aluminum ($Al(CH_3)_3$) (TMA hereinafter), silane (SiH_4), and diethyl zinc (DEZ hereinafter).

The sapphire substrate 1 of single crystal, with its principal crystal plane (a-surface $\{11\bar{2}0\}$) cleaned by solvent washing and heat treatment, was set on the susceptor placed in a reaction chamber of an MOVPE apparatus.

The sapphire substrate 1 underwent vapor phase etching at 1100 °C with H_2 flowing through the reaction chamber at a flow rate of 2 l/min under normal pressure.

On the sapphire substrate 1 was formed the AlN buffer layer 2 (about 500 Å thick) at 400 °C by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, and TMA at a flow rate of 1.8×10^{-5} mol/min.

On the buffer layer 2 was formed the n^+-layer 3 of high carrier concentration ($1.5 \times 10^{18}/cm^3$) of 2.2 μm thick GaN by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, TMG at a flow rate of 1.7×10^{-4} mol/min, and silane (diluted to 0.86 ppm with H_2) at a flow rate of 200 ml/min, with the sapphire substrate 1 kept at 1150 °C.

On the n^+-layer 3 was formed the n-layer 4 of low carrier concentration ($1 \times 10^{15}/cm^3$) of 1.5 μm

thick GaN by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, and TMG at a flow rate of 1.7×10^{-4} mol/min, with the sapphire substrate 1 kept at 1150 °C.

On the n-layer 4 was formed the i-layer 6 of 0.2 μm thick GaN by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, TMG at a flow rate of 1.7×10^{-4} mol/min, and DEZ at a flow rate of 1.5×10^{-4} mol/min, with the sapphire substrate 1 kept at 900 °C.

Thus there was obtained the multi-layer structure as shown in Fig. 2.

On the i-layer 6 was formed a 2000 Å thick SiO_2 layer 11 by sputtering as shown in Fig. 3. On the SiO_2 layer 11 was formed a photoresist layer 12 which subsequently underwent a photolithographic processing to make a pattern corresponding to a figure of the electrode connected to the n^+-layer 3.

The exposed part (not covered by the photoresist layer 12) of the SiO_2 layer 11 underwent etching with hydrofluoric acid for its removal, as shown in Fig. 4.

The exposed part (not covered by the photoresist layer 12 and the SiO_2 layer 11) of the i-layer 6 underwent dry etching with CCl_2F_2 gas at a flow rate of 10 cc/min and a high-frequency electric power of 0.44

W/cm^2 in a vacuum of 0.04 Torr and subsequently underwent dry etching with argon. The dry etching removed not only the exposed part of the i-layer 6 but also the n-layer 4 and the upper part of the n^+-layer 3 which are underneath the exposed part of the i-layer 6, as shown in Fig. 5.

The SiO_2 layer 11 remaining on the i-layer 6 was removed with hydrofluoric acid as shown in Fig. 6.

On the entire surface of the sample was formed an Al layer 13 by vapor deposition as shown in Fig. 7. On the Al layer 13 was formed a photoresist layer 14 which subsequently underwent the photolithographic processing to make a pattern corresponding to a figure of the electrodes connected to the n^+-layer 3 and the i-layer 6, respectively.

The exposed part (not covered by the photoresist layer 14) of the Al layer 13 underwent etching with nitric acid as shown in Fig. 7. The photoresist 14 was removed with acetone. Thus there were formed the electrode 8 for the n^+-layer 3 and the electrode 7 for the i-layer 6.

Such an above-mentioned process could make a gallium nitride light-emitting element of MIS (metal-insulator-semiconductor) structure as shown in Fig. 1.

The thus obtained light-emitting diode 10 was

found to have a luminous intensity of 0.2 mcd. This value is 4 times higher than that of the conventional light-emitting diode which is composed simply of an i-layer with impurity concentration of 2 x 10^{20} /cm^3 and a 4 μm thick n-layer with carrier concentration of 5 x 10^{17}/cm^3.

In addition, the inspection of the luminescent surface revealed that the number of luminescent points is much greater than that of the conventional light-emitting diode.

Several samples were prepared in the same manner as mentioned above except that the carrier concentration in the n-layer of low carrier concentration was varied, and they were tested for luminous intensity and emission spectrum. The results are shown in Fig. 8. It is noted that the luminous intensity decreases and the emission spectrum shifts to the red side according as the carrier concentration increases. This effect is estimated to be caused by that atoms of silicon as doping atoms diffuse or mix into the i-layer 6 as impurity atoms.

Example 2

In Fig. 9 there is shown a light-emitting diode 10 which has a sapphire substrate 1 on which is formed a 500 Å thick AlN buffer layer 2. On the buffer layer 2 are consecutively formed a 4 μm thick GaN n-layer 3

with carrier concentration of 5 x $10^{17}/cm^3$, an i_L-layer 5 of low impurity concentration of 5 x $10^{19}/cm^3$ of Zn, and an i_H-layer 6 of high impurity concentration (2 x $10^{20}/cm^3$ of Zn) . To the i_H-layer 6 and n-layer 3 are connected aluminum electrodes 7 and 8, respectively.

This light-emitting diode 10 was produced by the MOVPE.

The gases employed in this process are NH_3, H_2 (as carrier gas), trimethyl gallium TMG , trimethyl aluminum TMA, and diethyl zinc DEZ.

The sapphire substrate 1 of single crystal, with its principal crystal plane (c-surface ‹0001›) cleaned by solvent washing and heat treatment, was set on the susceptor placed in the reaction chamber of the MOVPE apparatus.

The sapphire substrate 1 underwent vapor phase etching at 1100 °C with H_2 flowing through the reaction chamber at a flow rate of 2 l/min under normal pressure.

On the sapphire substrate 1 was formed the AlN buffer layer 2 (about 500 Å thick) at 400 °C by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, and TMA at a flow rate of 1.8 x 10^{-5} mol/min.

On the buffer layer 2 was formed the 4 μm thick GaN n-layer 3 with carrier concentration of 1.5 x $10^{17}/cm^3$ by supplying H_2 at a flow rate of 20 l/min,

NH_3 at a flow rate of 10 l/min, and TMG at a flow rate of 1.7×10^{-4} mol/min with stopping the feeding of TMA, with the sapphire substrate 1 kept at 1150 °C.

On the n-layer 3 was formed the 0.2 μm thick GaN i_L-layer 5 of low impurity concentration ($5 \times 10^{19}/cm^3$ of Zn) by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, TMG at a flow rate of 1.7×10^{-4} mol/min, and DEZ at a flow rate of 1.5×10^{-4} mol/min, with the sapphire substrate 1 kept at 1000 °C.

On the i_L-layer 5 was formed the 0.2 μm thick GaN i_H-layer 6 of high impurity concentration ($2 \times 10^{20}/cm^3$ of Zn) by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, TMG at a flow rate of 1.7×10^{-4} mol/min, and DEZ at a flow rate of 1.5×10^{-4} mol/min, with the sapphire substrate 1 kept at 900 °C.

Thus there was obtained the multi-layer structure as shown in Fig. 10.

On the i_H-layer 6 was formed the 2000 Å thick SiO_2 layer 11 by sputtering as shown in Fig. 11. On the SiO_2 layer 11 was formed a photoresist layer 12 which subsequently underwent the photolithographic processing to make a pattern corresponding to the figure of the electrode connected to the n-layer 3.

The exposed part (not covered by the photoresist layer 12) of the SiO_2 layer 11 underwent etching with hydrofluoric acid for its removal, as shown in Fig. 12.

The exposed part (not covered by the photoresist layer 12 and the SiO_2 layer 11) of the i_H-layer 6 underwent dry etching with CCl_2F_2 gas at a flow rate of 10 cc/min and a high-frequency electric power of 0.44 W/cm2 in a vacuum of 0.04 Torr and subsequently underwent dry etching with argon. The dry etching removed not only the exposed part of the i_H-layer 6 but also the i_L-layer 5 and the upper part of the n-layer 3 which are underneath the exposed part of the i_H-layer 6, as shown in Fig. 13.

The SiO_2 layer 11 remaining on the i_H-layer 6 was removed with hydrofluoric arid as shown in Fig. 14.

On the entire surface of the sample was formed an Al layer 13 by vapor deposition as shown in Fig. 15. On the Al layer 13 was formed the photoresist layer 14 which subsequently underwent the photolithographic processing to make a pattern corresponding to the figure of the electrodes connected to the n-layer 3 and the i_H-layer 6, respectively.

The exposed part (not covered by the photoresist layer 14) of the Al layer 13 underwent etching with nitric acid as shown in Fig. 15. The photoresist 14 was

removed with acetone. Thus there were formed the electrode 8 for the n-layer 3 and the electrode 7 for the i_H-layer 6.

Such an above-mentioned process could make a gallium nitride light-emitting element of MIS structure as shown in Fig. 9.

The thus obtained light-emitting diode 10 was found to have a luminous intensity of 0.2 mcd. This value is 4 times higher than that of the conventional light-emitting diode which is composed simply of a 0.2 μm thick i-layer with impurity concentration of 2 x $10^{20}/cm^3$ and a 4 μm thick n-layer with carrier concentration of 5 x $10^{17}/cm^3$.

In addition, the inspection of the luminescent surface revealed that the number of luminescent points is much greater than that of the conventional light-emitting diode.

Several samples were prepared in the same manner as mentioned above except that the impurity concentration in the i_H-layer 6 of high impurity concentration was varied, and they were tested for luminous intensity and emission spectrum. The results are shown in Fig. 16. It is noted that the luminous intensity has a peak value and the emission spectrum shifts to a longer wavelength side when the impurity

concentration increases.

Example 3

In Fig. 17 there is shown a light-emitting diode 10 which has a sapphire substrate 1 on which is formed a 500 Å thick AlN buffer layer 2. On the buffer layer 2 are consecutively formed a 2.2 μm thick GaN n^+-layer 3 of high carrier concentration ($1.5 \times 10^{18}/cm^3$), a 1.5 μm thick GaN n-layer 4 of low carrier concentration ($1 \times 10^{15}/cm^3$), an i_L-layer 5 of low impurity concentration ($5 \times 10^{19}/cm^3$ of Zn), and an i_H-layer 6 of high impurity concentration ($2 \times 10^{20}/cm^3$ of Zn) . To the i_H layer 6 and n^+-layer 3 are connected aluminum electrodes 7 and 8, respectively. This light-emitting diode 10 was produced by the MOVPE with organometal compound in the following manner.

The gases employed in this process are NH_3, H_2 (as carrier gas), trimethyl gallium ($Ga(CH_3)_3$) (TMG), trimethyl aluminum ($Al(CH_3)_3$) (TMA) ,silane (SiH_4), and diethyl zinc (DEZ).

The sapphire substrate 1 of single crystal, with its principal crystal plane (c-surface ⟨0001⟩) cleaned by solvent washing and heat treatment, was set on the susceptor placed in the reaction chamber of the MOVPE apparatus.

The sapphire substrate 1 underwent vapor phase

etching at 1100 °C with H_2 flowing through the reaction chamber at a flow rate of 2 l/min under normal pressure.

On the sapphire substrate 1 was formed the AlN buffer layer 2 (about 500 Å thick) at 400 °C by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, and TMA at a flow rate of 1.8×10^{-5} mol/min.

On the buffer layer 2 was formed the 2.2 μm thick GaN n^+-layer 3 of high carrier concentration ($1.5 \times 10^{18}/cm^3$) by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, TMG at a flow rate of 1.7×10^{-4} mol/min, and silane (diluted to 0.86 ppm with H_2) at a flow rate of 200 ml/min for 30 minutes, with the sapphire substrate 1 kept at 1150 °C.

On the n^+-layer 3 was formed the 1.5 μm thick GaN n-layer 4 of low carrier concentration (1×10^{15} $/cm^3$) by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, and TMG at a flow rate of 1.7×10^{-4} mol/min, with the sapphire substrate 1 kept at 1150 °C.

On the n-layer 4 was formed the 0.2 μm thick GaN i_L-layer 5 of low impurity concentration ($5 \times 10^{19}/cm^3$ of Zn) by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, TMG at a flow rate of 1.7×10^{-4} mol/min, and DEZ at a flow rate of 1.5×10^{-4} mol/min, with the sapphire substrate 1 kept

at 1000°C.

On the i_L-layer 5 was formed the 0.2 μm thick GaN i_H-layer 6 of high impurity concentration (2 x $10^{20}/cm^3$ of Zn) by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, TMG at a flow rate of 1.7×10^{-4} mol/min, and DEZ at a flow rate of 1.5×10^{-4} mol/min, with the sapphire substrate 1 kept at 900°C.

Thus there was obtained the multi-layer structure as shown in Fig. 18.

On the i_H-layer 6 was formed the 2000 Å thick SiO_2 layer 11 by sputtering as shown in Fig. 19. On the SiO_2 layer 11 was formed a photoresist layer 12 which subsequently underwent the photolithographic processing to make a pattern for the electrode connected to the n^+-layer 3.

The exposed part (not covered by the photoresist layer 12) of the SiO_2 layer 11 underwent etching with hydrofluoric acid for its removal, as shown in Fig. 20.

The exposed part (not covered by the photoresist layer 12 and the SiO_2 layer 11) of the i_H-layer 6 underwent dry etching with CCl_2F_2 gas at a flow rate of 10 cc/min and a high-frequency electric power of 0.44 W/cm^2 in a vacuum of 0.04 Torr and subsequently underwent dry etching with argon. The dry etching

removed not only the exposed part of the i_H-layer 6 but also the i_L-layer 5 and the n-layer 4 and the upper part of the n^+-layer 3 which are underneath the exposed part of the i_H-layer 6, as shown in Fig. 21.

The SiO_2 layer 11 remaining on the i_H-layer 6 was removed with hydrofluoric arid as shown in Fig. 22.

On the entire surface of the sample was formed an Al layer 13 by vapor deposition as shown in Fig. 23. On the Al layer 13 was formed the photoresist layer 14 which subsequently underwent the photolithographic processing to make a pattern for the electrodes connected to the n^+-layer 3 and the i_H-layer 6, respectively.

The exposed part (not covered by the photoresist layer 14) of the Al layer 13 underwent etching with nitric acid as shown in Fig. 23. The photoresist 14 was removed with acetone. Thus there were formed the electrode 8 for the n^+-layer 3 and the electrode 7 for the i_H-layer 6.

Such an above-mentioned process could make a gallium nitride light-emitting element of MIS structure as shown in Fig. 17.

The thus obtained light-emitting diode 10 was found to have a luminous intensity of 0.4 mcd. This value is 8 times higher than that of the conventional

light-emitting diode which is composed simply of a 0.2 μm thick i-layer with impurity concentration of 2 x $10^{20}/cm^3$ and a 4 μm thick n-layer with a carrier concentration of 5 x $10^{17}/cm^3$.

In addition, the inspection of the luminescent surface revealed that the number of luminescent points is much greater than that of the conventional light-emitting diode.

Several samples were prepared in the same manner as mentioned above except that the carrier concentration in the n-layer 4 of low carrier concentration was varied, and they were tested for luminous intensity and emission spectrum. The results are shown in Fig. 24. It is noted that the luminous intensity decreases and the emission spectrum shifts to the red side according as the carrier concentration increases.

Also, several samples were prepared in the same manner as mentioned above except that the impurity concentration in the i_H-layer 6 of high impurity concentration was varied, and they were tested for luminous intensity and emission spectrum. The results are shown in Fig. 25. It is noted that the luminous intensity has a peak value and the emission spectrum shifts to a longer wavelength side when the impurity concentration increases.

Example 4

A light-emitting diode 10 of the same structure as in Example 1 was prepared in the same manner as in Example 1 according to the steps shown in Figs. 2 to 7. The resistivity of the n^+-layer 3 was varied in the range of 3×10^{-1} Ωcm to 8×10^{-3} Ωcm by changing the conditions of the vapor phase epitaxy for the n^+-layer 3 of high carrier concentration, as shown in Fig. 26. The vapor phase epitaxy was carried out by supplying H_2 at a flow rate of 20 l/min, NH_3 at a flow rate of 10 l/min, TMG-carrying H_2 at a flow rate of 100 cc/min, and H_2-diluted silane (0.86 ppm) at a flow rate of 10 cc/min to 300 cc/min. (The TMG-carrying H_2 was prepared by bubbling H_2 in TMG cooled at -15°C.)

In the above-mentioned case, the resistivity of the n^+-layer 3 was varied by changing the flow rate of silane, but it is also possible to achieve the same object by changing the flow rate of other raw material gases or by changing the mixing ratio of silane and other raw material gases.

In this example, silane was used as the Si dopant, but it can be replaced by an organosilicon compound such as tetraethylsilane ($Si(C_2H_5)_4$) in a gaseous state prepared by bubbling with H_2.

The process mentioned above permits one to

prepare the n^+-layer 3 of high carrier concentration and the n-layer 4 of low carrier concentration in such a manner that their resistivity can be controlled as desired.

The thus obtained light-emitting diode 10 was found to have a luminous intensity of 0.2 mcd. This value is 4 times higher than that of the conventional light-emitting diode which is composed simply of an i-layer and an n-layer. In addition, the inspection of the luminescent surface revealed that the number of luminescent points is much greater than that of the conventional light-emitting diode.

WHAT IS CLAIMED IS:

1. A light-emitting semiconductor device which comprises an n-layer of n-type gallium nitride compound semiconductor ($Al_xGa_{1-x}N$; inclusive of x=0) and an i-layer of insulating gallium nitride compound semiconductor ($Al_xGa_{1-x}N$; inclusive of x=0) doped with p-type impurities, wherein at least one of said n-layer and said i-layer is of double-layer structure, the respective layers of said double-layer structure having different concentrations.

2. A light-emitting semiconductor device as claimed in Claim 1, wherein said n-layer is of double-layer structure including an n-layer of low carrier concentration and an n^+-layer of high carrier concentration, the former being adjacent to said i-layer.

3. A light-emitting semiconductor device as claimed in Claim 1, wherein said i-layer is of double-layer structure including an i_L-layer of low impurity concentration containing p-type impurities in comparatively low concentration and an i_H-layer of high impurity concentration containing p-type impurities in comparatively high concentration, the former being

adjacent to said n-layer.

4. A light-emitting semiconductor device as claimed in Claim 1, wherein said n-layer is of double-layer structure including an n-layer of low carrier concentration and an n^+-layer of high carrier concentration, the former being adjacent to said i-layer, and said i-layer is of double-layer structure including an i_L-layer of low impurity concentration containing p-type impurities in comparatively low concentration and an i_H-layer of high impurity concentration containing p-type impurities in comparatively high concentration, the former being adjacent to said n-layer.

5. A light-emitting semiconductor device as claimed in Claim 1, wherein the thickness of said n-layer is 2.5 - 12 μm.

6. A light-emitting semiconductor device as claimed in Claim 1, wherein the carrier concentration of said n-layer is 1×10^{14} - 1×10^{19} /cm^3.

7. A light-emitting semiconductor device as claimed in Claim 2, wherein the thickness of said n-

layer of low carrier concentration is 0.5 - 2 μm and the thickness of said n^+-layer of high carrier concentration is 2 - 10 μm.

8. A light-emitting semiconductor device as claimed in Claim 2, wherein the carrier concentration of said n-layer of low carrier concentration is 1×10^{14} - 1×10^{17} /cm^3 and the carrier concentration of said n^+-layer of high carrier concentration is 1×10^{17} - 1×10^{19} /cm^3.

9. A light-emitting semiconductor device as claimed in Claim 1, wherein the thickness of said i-layer is 0.03 - 1.3 μm.

10. A light-emitting semiconductor device as claimed in Claim 1, wherein the impurity concentration of said i-layer is 1×10^{16} - 5×10^{20} /cm^3.

11. A light-emitting semiconductor device as claimed in Claim 3, wherein the thickness of said i_L-layer of low impurity concentration is 0.01 - 1 μm and the thickness of said i_H-layer of high impurity concentration is 0.02 - 0.3 μm.

12. A light-emitting semiconductor device as claimed in Claim 3, wherein the impurity concentration of said i_L-layer of low impurity concentration is $1 \times 10^{16} - 5 \times 10^{19}$ /cm^3 and the impurity concentration of said i_H-layer of high impurity concentration is $1 \times 10^{19} - 5 \times 10^{20}$ /cm^3.

13. A light-emitting semiconductor device as claimed in Claim 2, wherein said n^+-layer of high carrier concentration is doped with silicon.

14. A light-emitting semiconductor device as claimed in Claim 4, wherein said n^+-layer of high carrier concentration is doped with silicon.

15. A light-emitting semiconductor device as claimed in Claim 3, wherein both said i_L-layer of low impurity concentration and said i_H-layer of high impurity concentration are doped with zinc, the amount of doped zinc in said i_H-layer of high impurity concentration being higher than that in said i_L-layer of low impurity concentration.

16. A light-emitting semiconductor device as claimed in Claim 4, wherein both said i_L-layer of low impurity concentration and said i_H-layer of high

impurity concentration are doped with zinc, the amount of doped zinc in said i_H-layer of high impurity concentration being higher than that in said i_L-layer of low impurity concentration.

17. A method for producing a light-emitting semiconductor device comprising an n-layer of n-type gallium nitride compound semiconductor ($Al_XGa_{1-X}N$; inclusive of x=0) and an i-layer of insulating gallium nitride compound semiconductor ($Al_XGa_{1-X}N$; inclusive of x=0) doped with p-type impurities from organometal compound by vapor phase epitaxy, comprising the steps of:

feeding a silicon-containing gas and other raw material gases together at a controlled mixing ratio to a substrate; and

growing said n-layer having a controlled conductivity.

18. A method as claimed in Claim 17, comprising:

growing an n^+-layer of high carrier concentration, which is an n-type gallium nitride compound semiconductor ($Al_XGa_{1-X}N$; inclusive of x=0) having a comparatively high conductivity, on said substrate

having a buffer layer of aluminum nitride formed thereon, by feeding said silicon-containing gas and said other raw material gases together at a controlled mixing ratio; and

growing an n-layer of low carrier concentration, which is an n-type gallium nitride compound semiconductor ($Al_xGa_{1-x}N$; inclusive of x=0) having a comparatively low conductivity, on said n^+-layer, by feeding said raw material gases excluding said silicon-containing gas.

ABSTRACT OF THE DISCLOSURE

Disclosed herein are (1) a light-emitting semiconductor device that uses a gallium nitride compound semiconductor ($Al_XGa_{1-X}N$) in which the n-layer of n-type gallium nitride compound semiconductor ($Al_XGa_{1-X}N$) is of double-layer structure including an n-layer of low carrier concentration and an n^+-layer of high carrier concentration, the former being adjacent to the i-layer of insulating gallium nitride compound semiconductor ($Al_XGa_{1-X}N$); (2) a light-emitting semiconductor device of similar structure as above in which the i-layer is of double-layer structure including an i_L-layer of low impurity concentration containing p-type impurities in comparatively low concentration and an i_H-layer of high impurity concentration containing p-type impurities in comparatively high concentration, the former being adjacent to the n-layer; (3) a light-emitting semiconductor device having both of the above-mentioned features and (4) a method of producing a layer of an n-type gallium nitride compound semiconductor ($Al_XGa_{1-X}N$) having a controlled conductivity from an organometallic compound by vapor phase epitaxy, by feeding a silicon-containing gas and other raw material gases together at a controlled mixing ratio.

FIG. 1

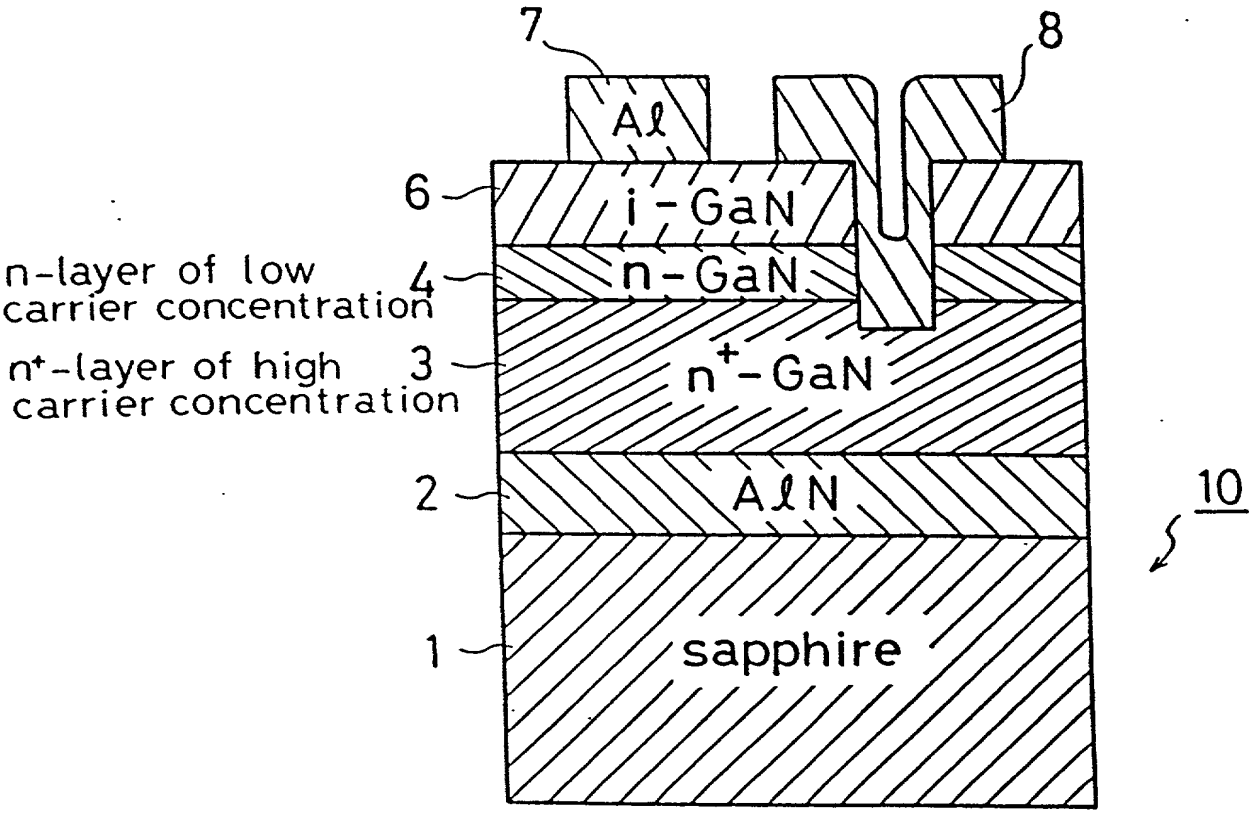

7
8
Al
6
i-GaN
n-layer of low carrier concentration
4
n-GaN
n+-layer of high carrier concentration
3
n+-GaN
2
AlN
10
1
sapphire

FIG.2

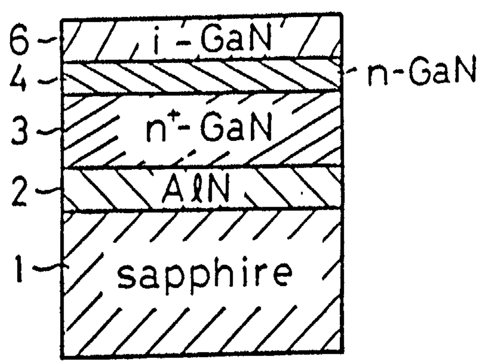


FIG.3

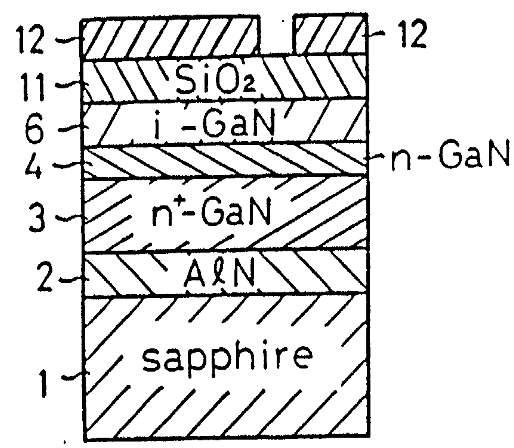


FIG.4

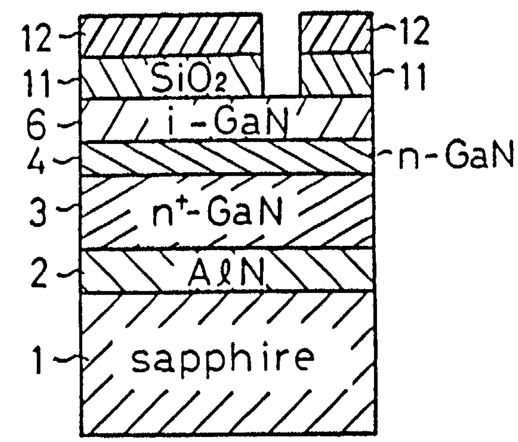


FIG.5

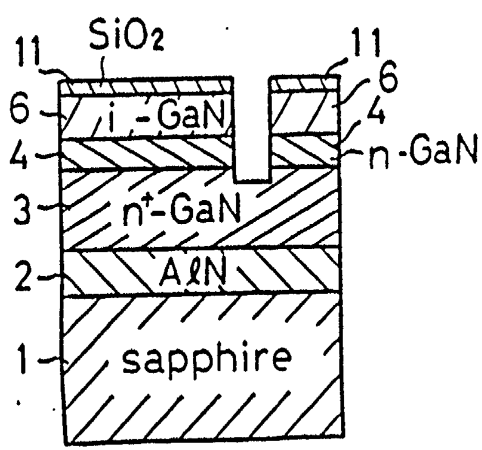


FIG.6

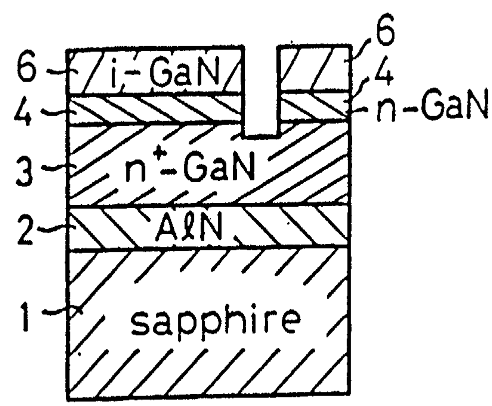


FIG.7

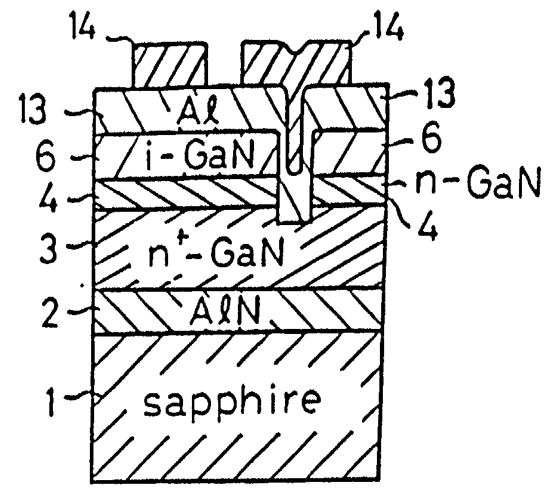


FIG. 8

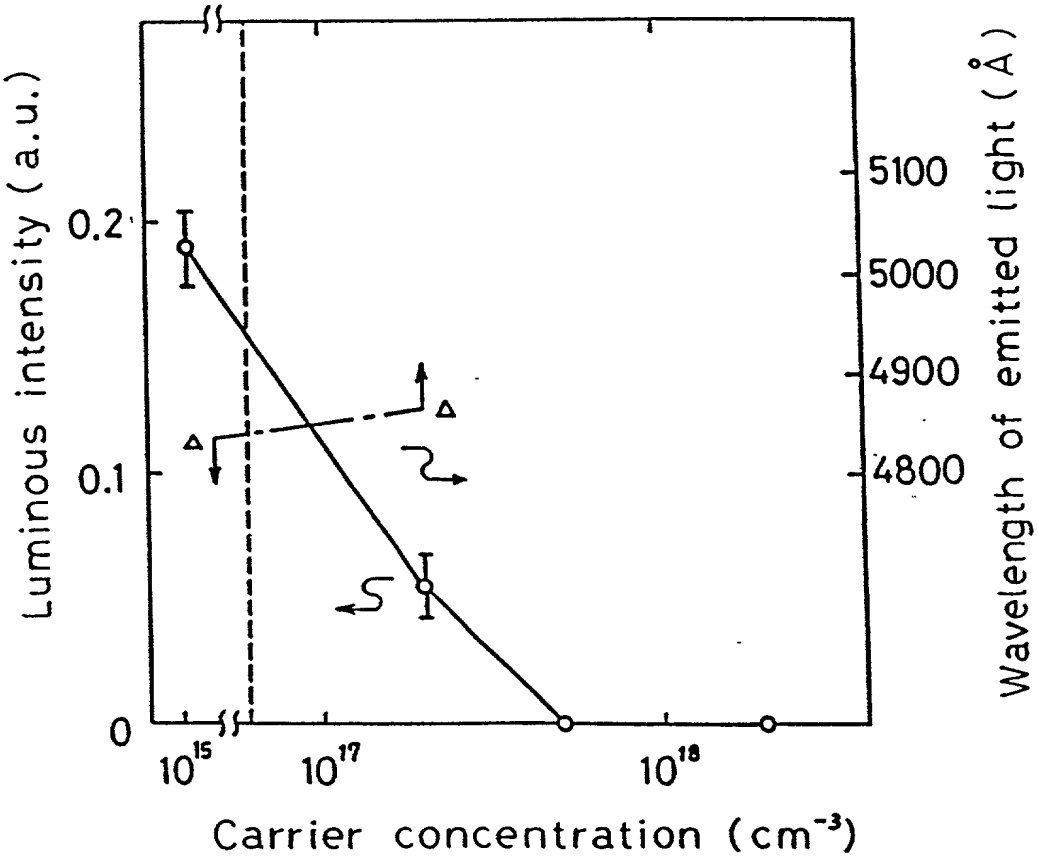

Luminous intensity (a.u.)
0.2
0.1
0
10^{15}
10^{17}
10^{18}
Carrier concentration (cm^{-3})
5100
5000
4900
4800
Wavelength of emitted light (Å)

FIG. 9

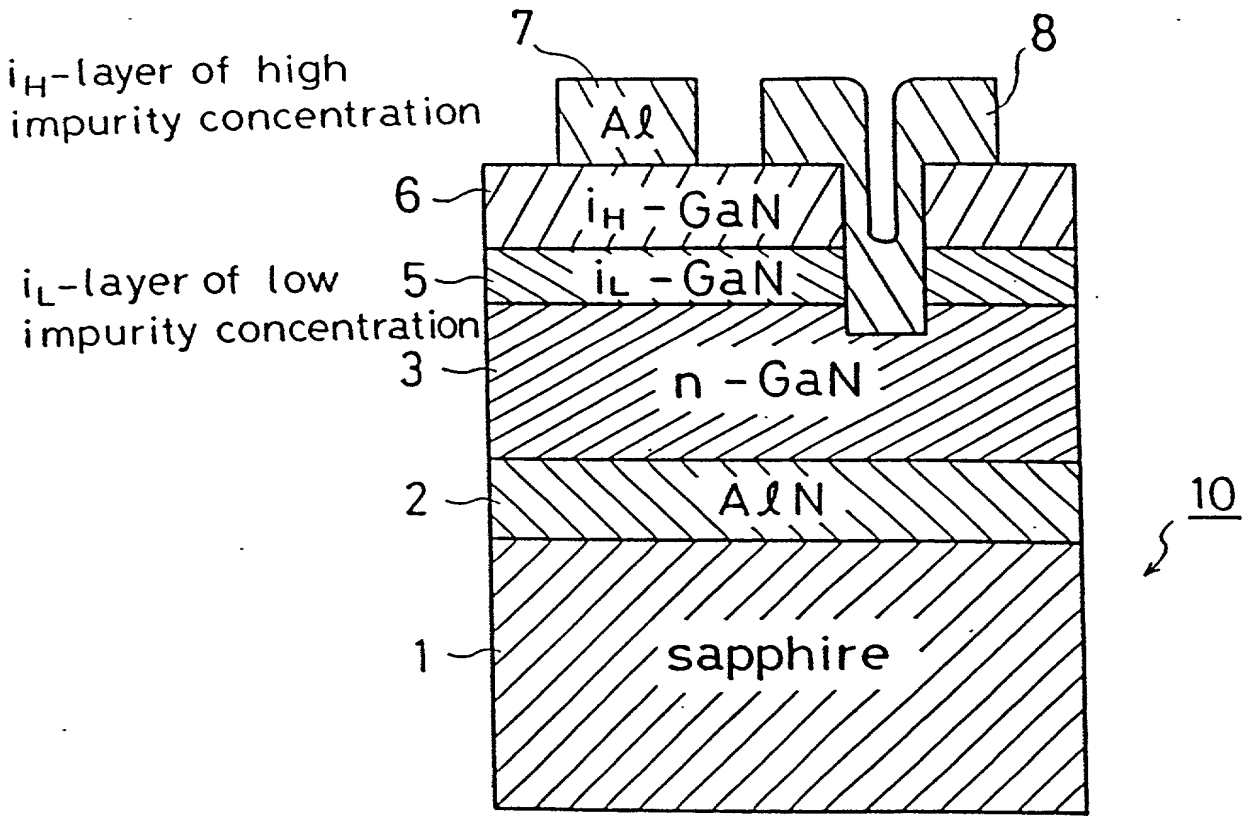

i_H-layer of high impurity concentration
i_L-layer of low impurity concentration
7
8
Aℓ
6
i_H-GaN
5
i_L-GaN
3
n-GaN
2
AℓN
1
sapphire
10

FIG.10

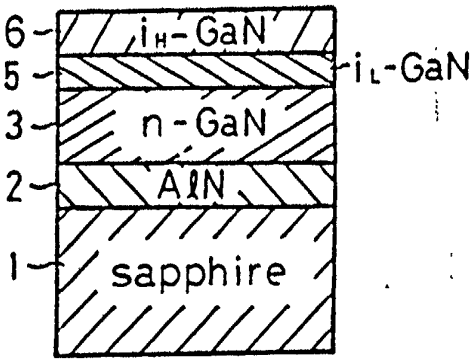


FIG.11

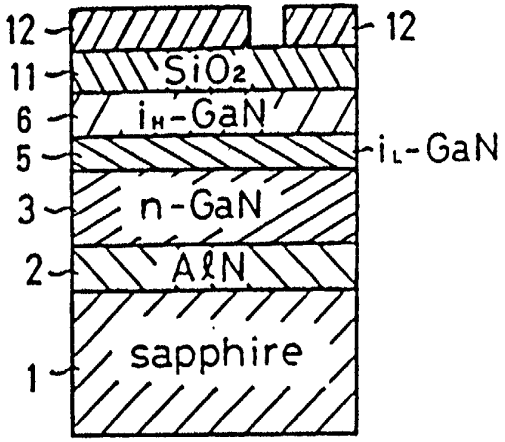


FIG.12

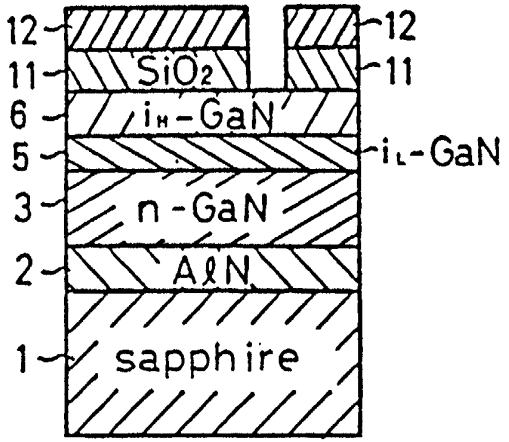


FIG.13

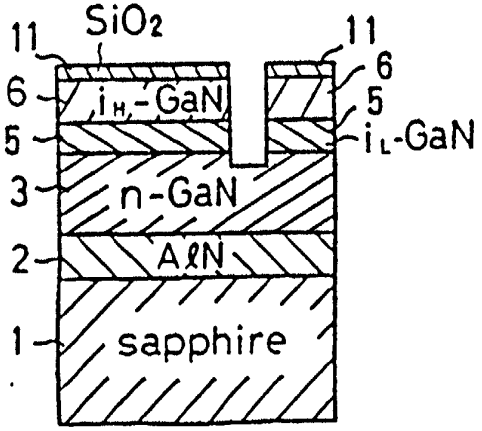


FIG.14

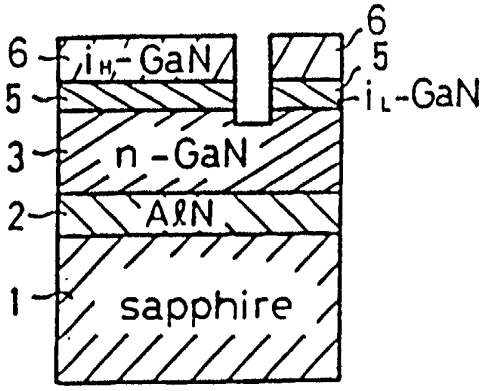


FIG.15

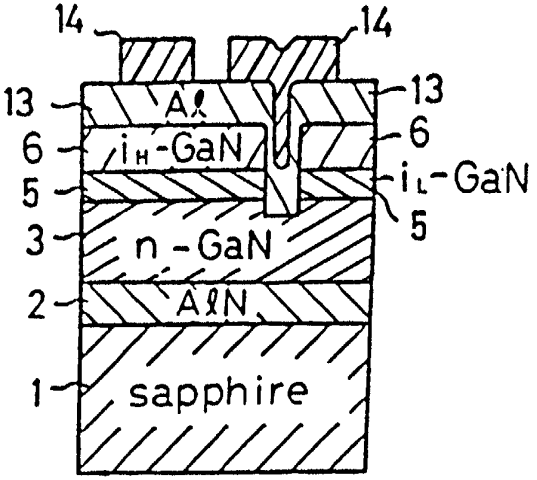


FIG. 16

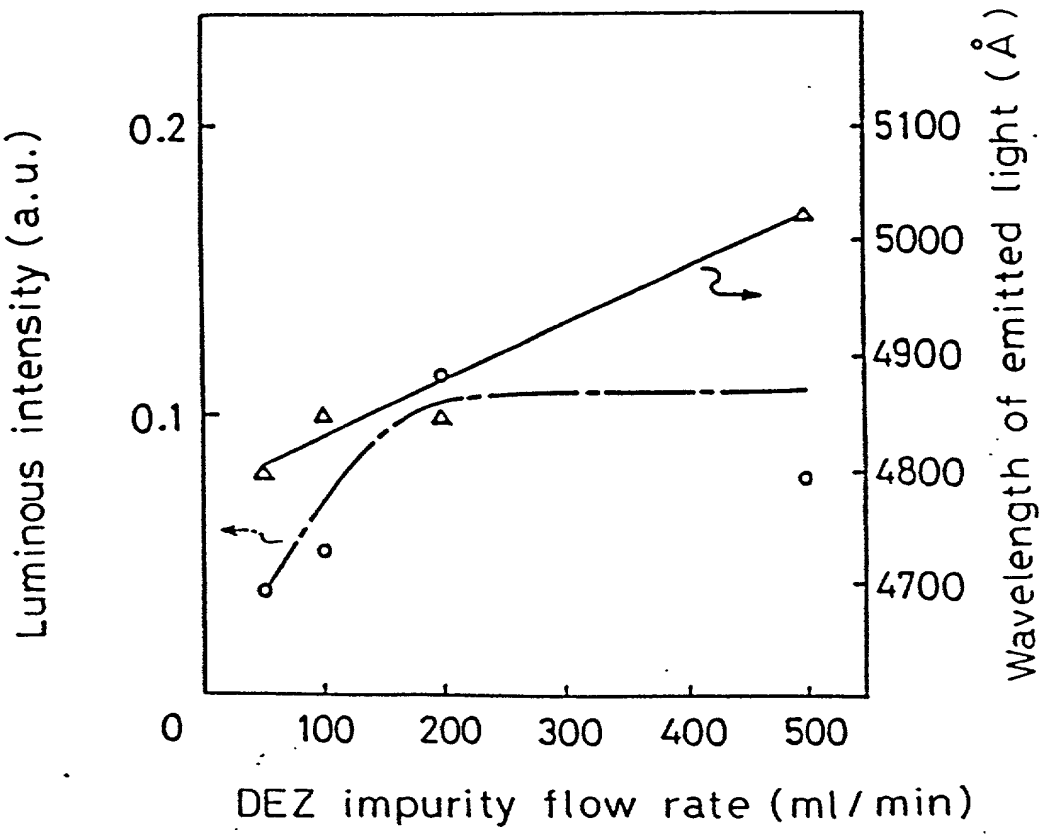

Luminous intensity (a.u.)
0.2
0.1
0
100
200
300
400
500
DEZ impurity flow rate (ml/min)
5100
5000
4900
4800
4700
Wavelength of emitted light (Å)

FIG. 17

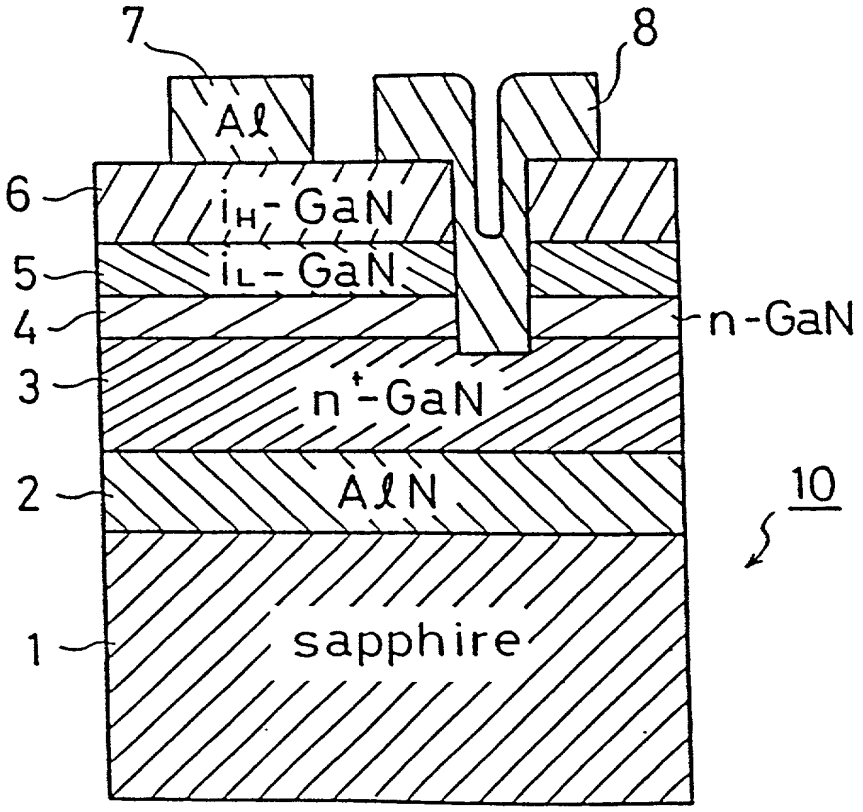


FIG. 18

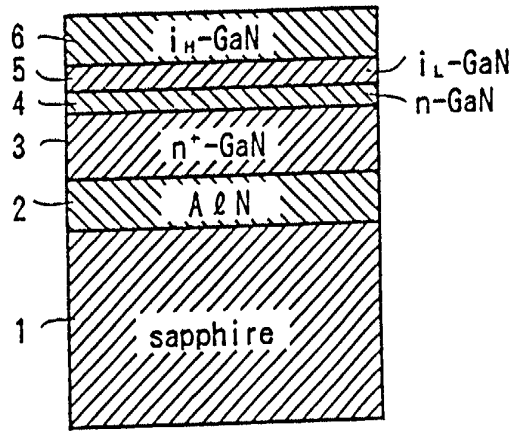


FIG. 19

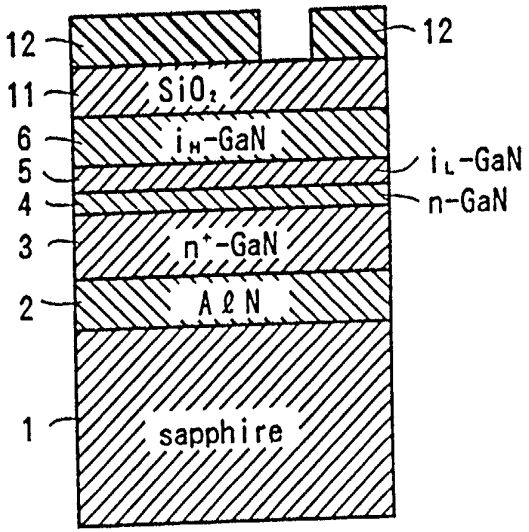


FIG. 20

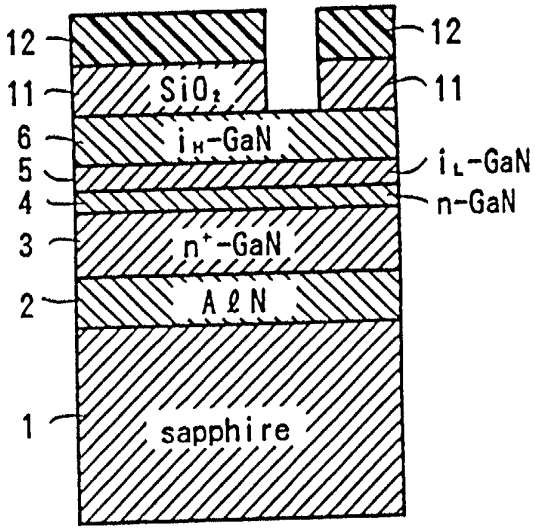


FIG. 21

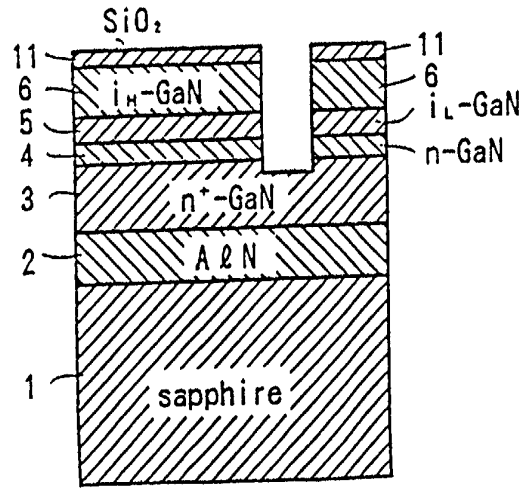


FIG. 22

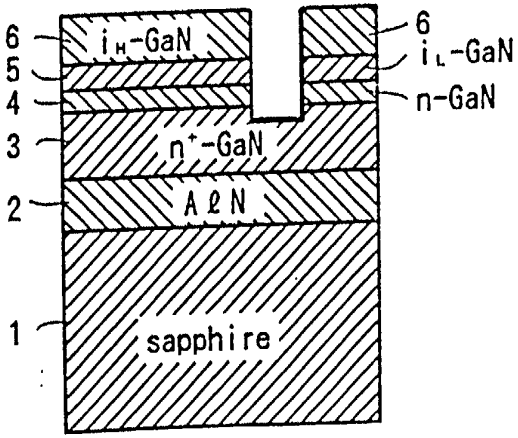


FIG. 23

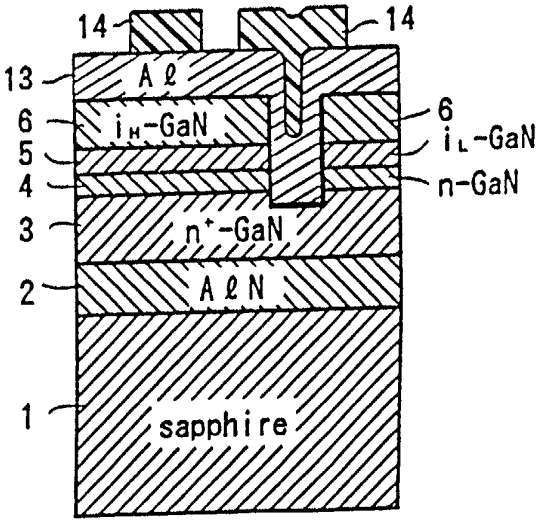


FIG. 24

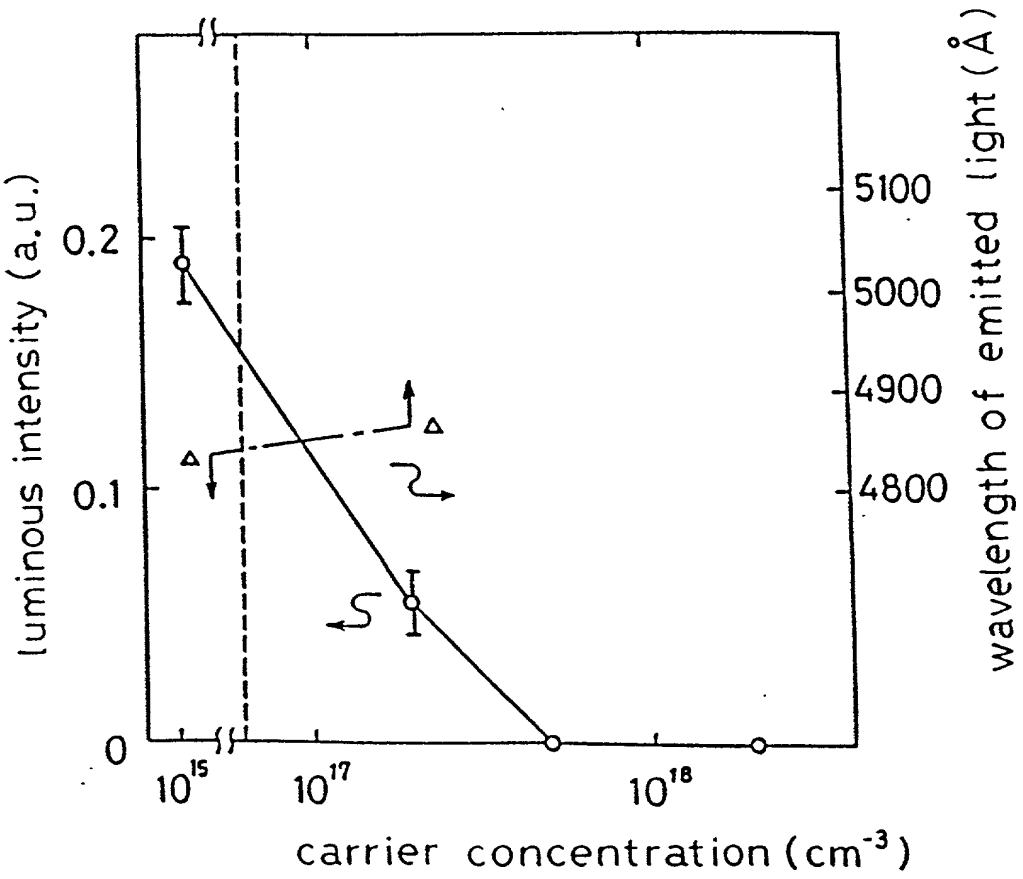

luminous intensity (a.u.)
0.2
0.1
0
5100
5000
4900
4800
wavelength of emitted light (Å)
10^{15}
10^{17}
10^{18}
carrier concentration (cm^{-3})

FIG. 25

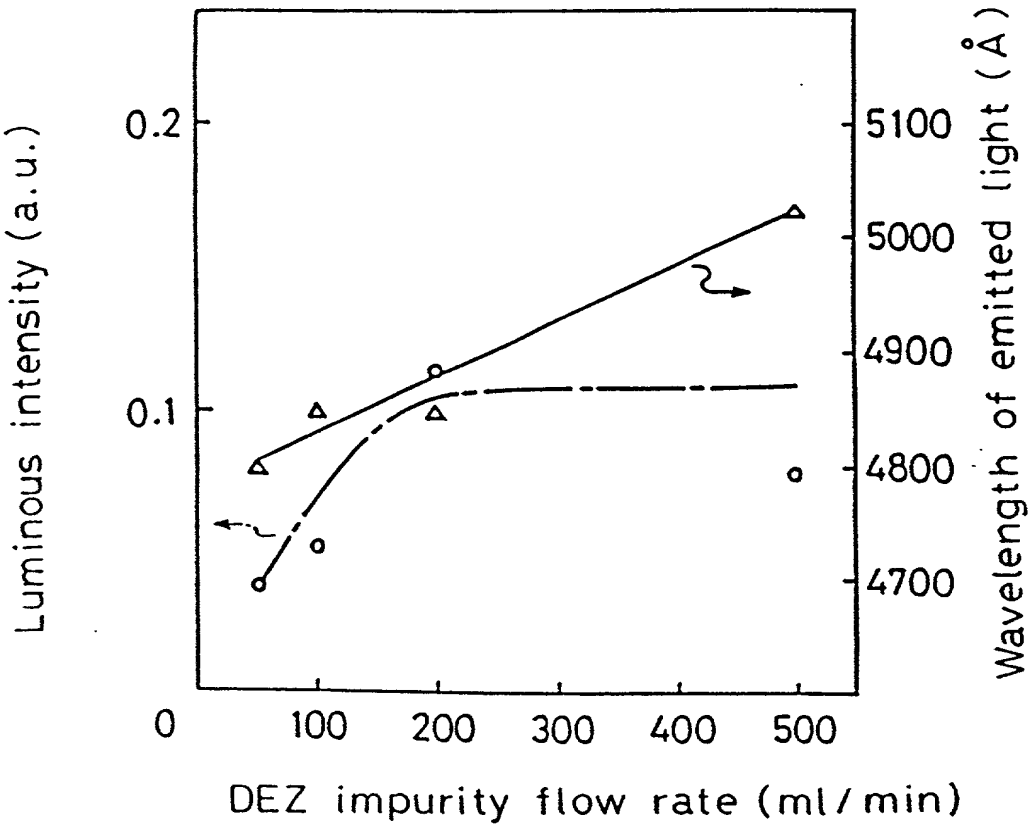
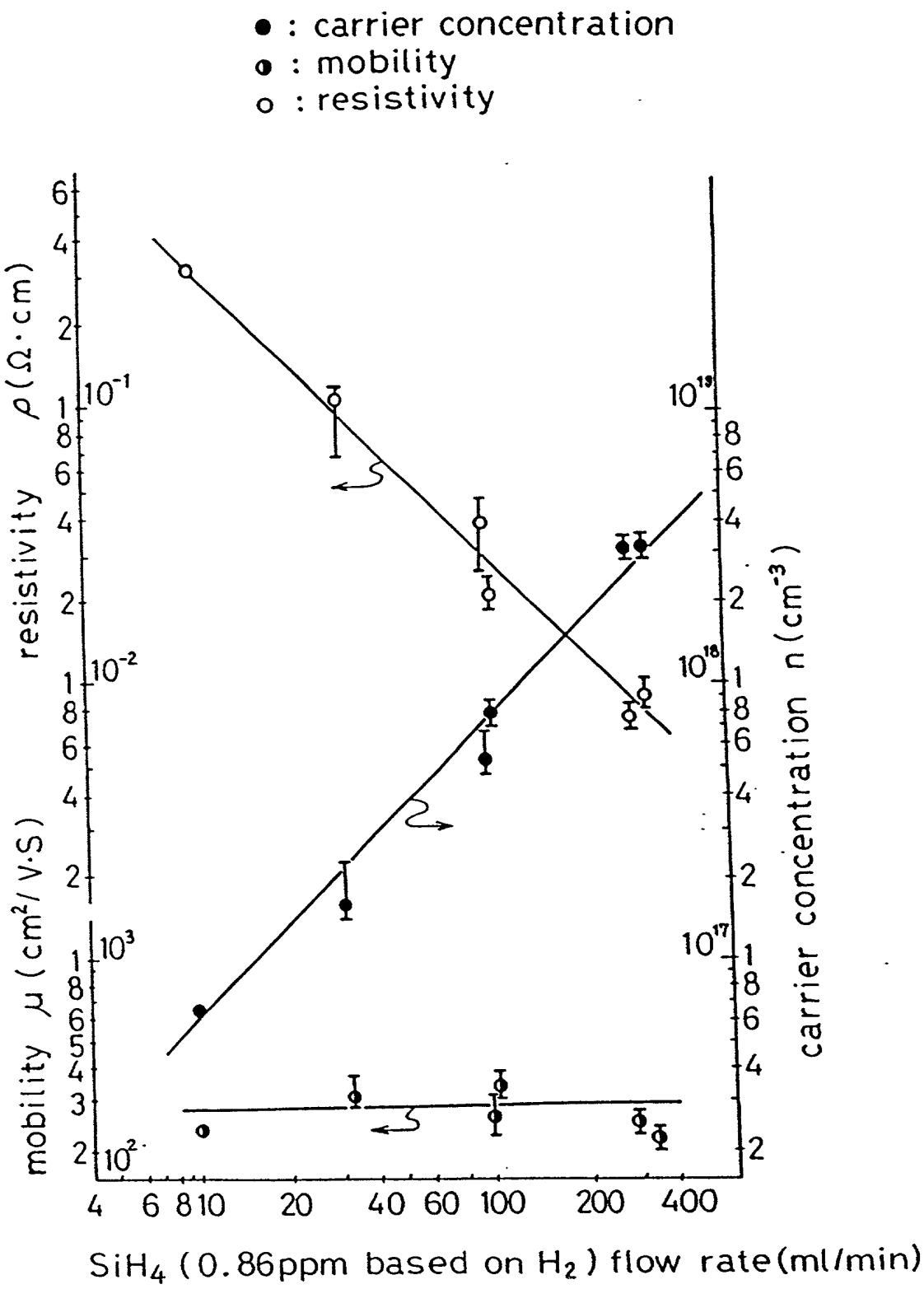

Luminous intensity (a.u.)
0.2
0.1
0
100
200
300
400
500
DEZ impurity flow rate (ml/min)
5100
5000
4900
4800
4700
Wavelength of emitted light (Å)

FIG. 26


● : carrier concentration
◐ : mobility
○ : resistivity
resistivity ρ(Ω·cm)
mobility μ(cm²/V·S)
carrier concentration n(cm⁻³)
SiH4 (0.86ppm based on H2) flow rate(ml/min)

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

CDC-1

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I lieve I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are lis below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

LIGHT-EMITTING SEMICONDUCTOR DEVICE USING GALLIUM NITRIDE GROUP COMPOUND

the specification of which (CHECK applicable BOX(ES)).

☐ is attached hereto.

☐ was filed on ..... as U.S. Application Serial No. .....

☐ was filed as PCT international Application No. PCT/...../..... on .....

and (if applicable to U.S. or PCT application) was amended on .....

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by s amendment referred to above, to the best of my ability. I acknowledge the duty to disclose information which is material to the examinat of this application in accordance with 37 C.F.R. 1.56(a) and 35 U.S.C. 102 both as set forth on the reverse side hereof. I hereby claim fore priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identi below any foreign application for patent or inventor's certificate having a filing date (1) before that of the application on which priority is claim or (2) if no priority claimed, before the filing date of this application:

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	Country	Day/MONTH/Year Filed	Yes	No
P050209/1990	Japan	28/02/1990	X	
P050210/1990	Japan	28/02/1990	X	
P050211/1990	Japan	28/02/1990	X	
P050212/1990	Japan	28/02/1990	X	

I hereby claim the benefit under 35 U.S.C. 120/365 of all United States and PCT international applications listed below and, insofar as the s ject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragrapl 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56(a) which occurred between the filing c of the prior applications and the national or PCT international filing date of this application:

PRIOR U.S. OR PCT APPLICATION(S)

Application Serial No.	Day/MONTH/Year Filed	Status: patented, pending, abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are lieved to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are p ishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements r jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Cushman, Darby & Cushman, Eleventh Floor, 1615 L Street, N.W., Washington, D.C. 20036, telephone number 861-3 (to whom all communications are to be directed), and the below named partners thereof (of the same address) individually and collectively attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the sulting patent.

Paul N. Kokulis	16773	Lawrence A. Hymo	19057	George M. Sirilla	18221	Watson T. Scott	26581
Allen Kirkpatrick	16749	Akin T. Davis	19973	William T. Bullinger	25503	Peter W. Gowdey	25872
George T. Mobille	17353	Edgar H. Martin	20534	Donald J. Bird	25323	Dale S. Lazar	28872
James L. Dooley	17710	William K. West, Jr.	22057	James R. Longacre	24421	Glenn J. Perry	28458
		Kevin E. Joyce	20508	W. Warren Taltavull	25647	Kendrew H. Colton	30368
Raymond F. Lippitt	17519	Edward M. Prince	22429	Michael L. Keller	26751		
G. Lloyd Knight	17698	Donald B. Deaver	23048	Charles R. Donohoe	24546		
Carl G. Love	18781	David W. Brinkman	20817				

1) INVENTOR'S SIGNATURE Katsuhide Manabe Date April 10, 1991
Inventor's Name (typed) Katsuhide (First) Manabe (Middle Initial) (Family Name) Japanese (Citizenship)
Residence (City) Ichinomiya (State/Foreign Country) Japan
Post Office Address (Include Zip Code) 50-6, Ipponmatsu, Menjo, Yamato-cho, Ichinamiya-shi, Aichi-ken, Japan

2) INVENTOR'S SIGNATURE Akira Mabuchi Date April 10, 1991
Inventor's Name (typed) Akira (First) Mabuchi (Middle Initial) (Family Name) Japanese (Citizenship)
Residence (City) Nagoya (State/Foreign Country) Japan
Post Office Address (Include Zip Code) 4-26, Taisho-cho, Nakamura-ku, Nagoya-shi, Aichi-ken, Japan

3) INVENTOR'S SIGNATURE Hisaki Kato Date April 10, 1991
Inventor's Name (typed) Hisaki (First) Kato (Middle Initial) (Family Name) Japanese (Citizenship)
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FOR ADDITIONAL INVENTORS, check box ☒ and attach sheet with same information and signature a date for each.

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CLARATION AND POWER OF ATTORN[illegible]
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

CDC-1
1-

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I b lieve I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are list below) of the subject matter which is claimed and for which a patent is sought on the invention entitled .....

.....

.....

the specification of which (CHECK applicable BOX(ES)).

☐ is attached hereto.

☐ was filed on ..... as U.S. Application Serial No. .....

☐ was filed as PCT international Application No. PCT/...../..... on .....

and (if applicable to U.S. or PCT application) was amended on .....

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by a amendment referred to above, to the best of my ability. I acknowledge the duty to disclose information which is material to the examinati of this application in accordance with 37 C.F.R. 1.56(a) and 35 U.S.C. 102 both as set forth on the reverse side hereof. I hereby claim forei priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identifi below any foreign application for patent or inventor's certificate having a filing date (1) before that of the application on which priority is claim or (2) if no priority claimed, before the filing date of this application:

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	Country	Day/MONTH/Year Filed	Yes	No

I hereby claim the benefit under 35 U.S.C. 120/365 of all United States and PCT international applications listed below and, insofar as the su ject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56(a) which occurred between the filing d of the prior applications and the national or PCT international filing date of this application:

PRIOR U.S. OR PCT APPLICATION(S)

Application Serial No.	Day/MONTH/Year Filed	Status: patented, pending, abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are lieved to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are p ishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements m jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Cushman, Darby & Cushman, Eleventh Floor, 1615 L Street, N.W., Washington, D.C. 20036, telephone number 861-3((to whom all communications are to be directed), and the below named partners thereof (of the same address) individually and collectively attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the sulting patent.

Paul N. Kokulis	16773	Lawrence A. Hymo	19057	George M. Sirilla	18221	Watson T. Scott	26581
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